Electrical Characteristics Analysis and Comparison between Through Silicon Via(TSV) and Through Glass Via(TGV)

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***Abstract*— The electrical characteristics of silicon and glass interposer channel are heavily affected by the design of through silicon via (TSV) and through glass via (TGV). In this paper, we analyzed the overall signal integrity of glass and silicon interposer channel including through package via. To compare electrical property between silicon and glass, we simulated these channels in frequency-domain and time-domain. We observed s-parameter of single and multiple via transition channel. Moreover we compared the characteristic impedance and eye diagram simulation results. Finally, we observed the change of electrical characteristics when the impedance mismatch is occurred at via pad.**

Keywords— Interposer, Through Silicon Via(TSV); Through Glass Via(TGV), 2.5D IC;

I. INTRODUCTION

Functional density of electronic systems have increased with highly miniaturized digital convergence. With this miniaturization trend in ICs, system integration technology also has been developed. Especially, advent of 3D/2.5D IC technology dramatically increased packaging density. Through package via (TPV), which is core technology of 3D/2.5D IC provides shorter interconnection length and shorter electrical delay of channel form package to package. It significantly improves performance of high density, high speed and low power system. Unfortunately, conventional package is the bottleneck of increasing I/O pins for wide bandwidth system. Interposer technology enable fine-pitch channel design to close a gap between very fine-pitch chip and loose-pitch conventional package.

Currently, silicon and glass have been widely employed for the interposer substrate material. Silicon is most often used in interposer fabrication due to fine pitch patterning and suitable CTE. However, it has high cost limits and shows significant signal loss because of conductivity of silicon. Even though the process of glass is not ready to be fine as silicon interposer, glass is in the spotlight as the potential material for interposer. Due to intrinsic electrical property of glass, glass channel has good electrical property at high frequency range. Also, manufacturing cost of glass is much lower than silicon on-chip metal process due to large panel fabrication. [1]

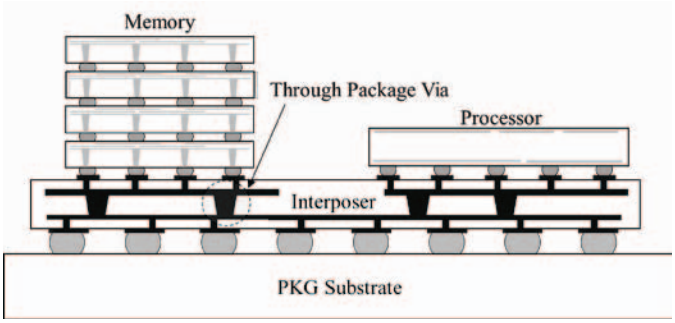
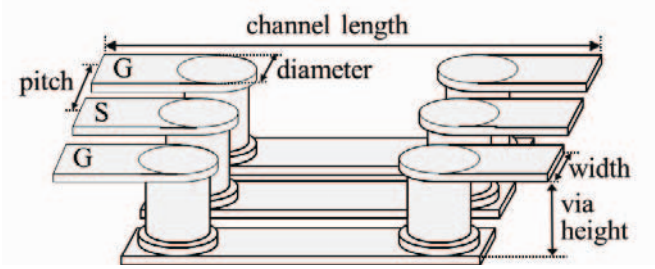


Figure 1. The concept of 2.5D IC with interposer and through package via

The electrical characteristics and performance of interposer channels are heavily affected by the interposer substrate material. Particularly, electrical properties of TGV are quite distinct from TSV even though their structural properties are similar. The oxide layer is formed to isolate the TSV from conductive silicon substrate. Oxide capacitance from insulation layer mainly affects the electrical property of TSV channel. There have been several focusing on the comparison of high speed interposer channel among silicon, glass and organic substrate.[2][3] However, the researches focusing on electrical property comparison between TSV and TGV are not enough. In this paper, we compared and analyzed the electrical characteristics of TSV and TGV using time-domain and frequency domain simulation.

II. SIMULATION SETUP



(a)

(b)

Figure 2. (a) The dimension of TSV and TGV channel for time-domain and frequency-domain simulation (b) Simulation setup for time-domain simulation

TABLE I. PHYSICAL PARAMETERS AND MATERIAL PROPERTIES OF SILICON AND GLASS CHANNEL FOR SIMULATION

Symbol	Interposer material	
	Silicon	***Glass***
Via diameter	32 μm	160μm
Line width	32μm	160μm
Via height	131μm	135μm
Pitch	300μm	300μm
Channel length	1.26mm	1.26mm
ε_rsub	11.2	5.3
σ_sub	10	-
tanδ	-	0.004

Structural parameters for glass and silicon channel are shown in figure. 2(a). For the fair comparison between TSV and TGV channel considering fine pitch silicon fabrication, we used stack-up from latest fabrication design rule of silicon and glass interposer. The stack-up of silicon interposer is referred to previous work.[4] It is composed of IMD layer, two silicon substrate layer, underfill layer and passivation layer. The design rule for glass interposer is determined by Packaging Research Center, Georgia Institute of Technology.

The value of physical parameters and material properties are summarized in table1. To observe the effect of through package via, all the lines are 50 ohm matched. The pitch of silicon and glass channel is same as 300μm. To minimize the reflection between line and via pad, line width and via pad diameter is designed as same value. In the final part, we change the proportion between via pad and line width to analyze effect of impedance mismatch at via pad. Differential GSSG channel is designed as same dimension of single-ended channel.

Simulation setup for interposer channel eye-diagram simulation is shown figure. 2(b). We used 50 ohm resistance for TX and RX part. Pseudo-random bit sequence 2^{31}-1 are injected with 50 ps rising and falling time. The data rate of input signal is 3.2Gbps and peak to peak amplitude of the signal is 1V.

III. ELECTRONICAL CHARACTERISTICS COMPARISON BETWEEN TSV AND TGV CHANNEL

A. Comparison of Single Via Transition TSV and TGV Channel

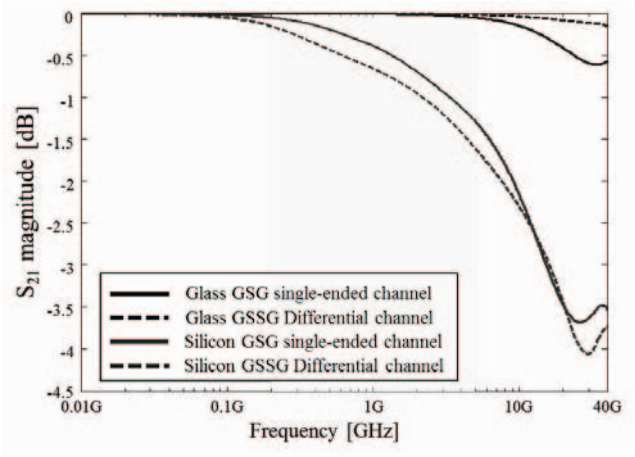


Figure 3. S_{21} magnitude of single-ended and differential TSV and TGV channel with single via transition

Insertion loss (S_{21}) of silicon and glass channel with single via transition is exported from full-3d simulation result. Overall length of two channels is same as 1.26mm and pitch is also same as 300μm. Insertion loss of silicon channel is much larger than that of glass channel. As frequency goes higher, insertion loss difference between two channels become bigger. Due to high conductivity of silicon substrate, loss of silicon channel increase as frequency increases. Whereas, insertion loss of glass channel shows reliably low value due to high resistivity of glass. S_{21} graph of silicon channel and glass channel both have small peak due to impedance mismatch at TSV and TGV. Because it is difficult to fabricate through package via with certain dimension, impedance mismatch is necessarily occurred. Glass channel has peak around 30GHz. The peak of silicon channel is located around 25GHz, lower frequency than glass channel. This peak is formed because the wave cannot pass through at certain frequency which is determined by material property and overall channel length. Because the relative permittivity of silicon substrate is bigger than glass, the peak of silicon channel is located at lower frequency than that of glass channel.

We compared differential TSV and TGV channel with single via transition which has the same pitch of single-ended channel. The differential signal TSV has larger effective capacitance and conductance from mutual terms. Therefore, in the frequency range under 5GHz, differential TSV shows larger insertion loss due to increase of oxide capacitance and substrate capacitance. Meanwhile, because of inductance dominant characteristic of TGV, increase of mutual capacitance improve signal integrity decreasing loss from impedance mismatch at TGV. [5] Differential channel can reduce loss from skew, crosstalk and ISI (Inter Symbol Interference), however we should carefully design the interposer channel because the loss can be increased depending on the channel design.

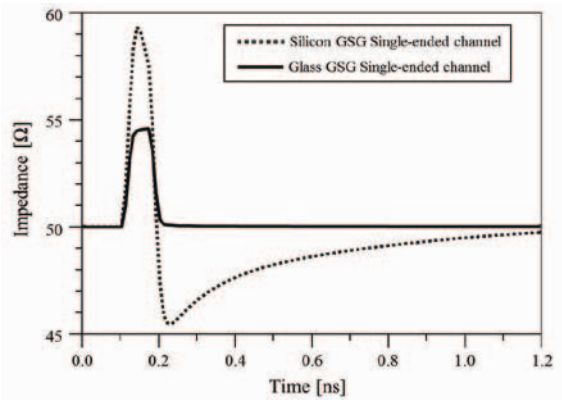


Figure 4. Characteristic impedance of single-ended TSV and TGV channel with single via transition

TDR (Time-domain Reflectometry) simulation result is shown in figure 4. Glass channel shows inductance dominant characteristic as reflections show greater than the 50Ohm. Refer to scalable TGV model, inductance of via is mostly dominant factor which determine electrical property of through glass via. Meanwhile, the characteristic impedance of TSV is dominated by the oxide capacitance between copper and conductive silicon substrate. TSV has both inductive and capacitive characteristic from via and oxide layer.

B. *Comparsion of Multiple Via Transition TSV and TGV Channel*

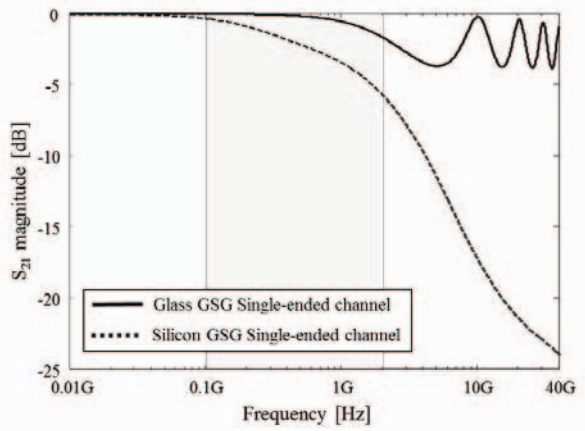
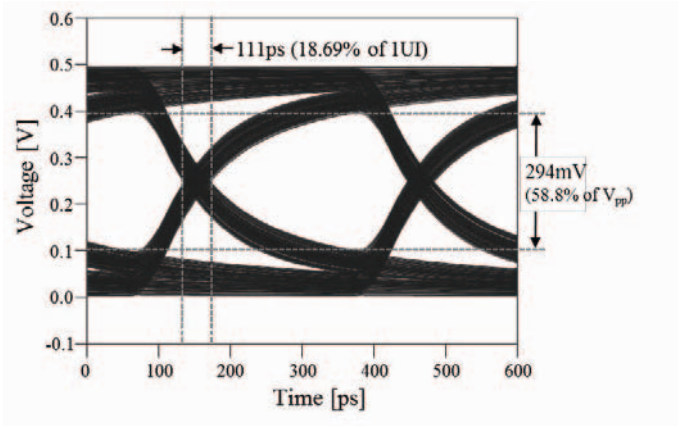


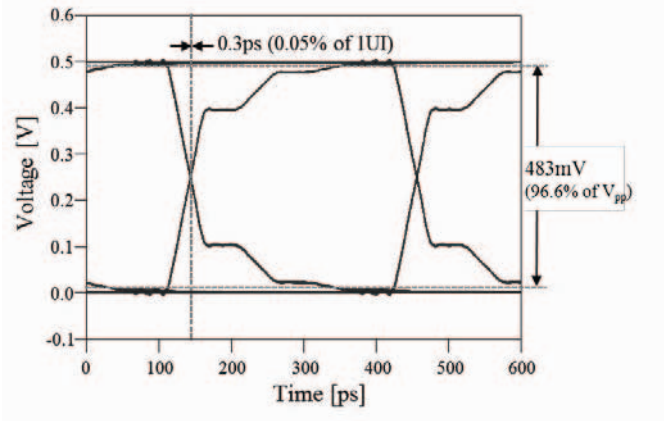
Figure 5. S_{21} magnitude of single-ended TSV and TGV channel with multiple via transition

We simulated and analyzed the silicon and glass interposer channel with multiple via transition. There are 8 via transition in this channel pattern and overall channel length is 10.08mm. Current flows through 16 TSVs and TGVs and 8mm GSG line. At the frequency of 40GHz, S21 magnitude of silicon channel is -23.96dB. The overall S21 level of glass channel is higher than that of silicon channel. Electrical property of silicon channel can be analyzed by categorizing the frequency range into three parts. Under 0.1GHz low frequency range, leakage through the conductive silicon substrate after passing through the insulator dominantly increases the insertion loss. In this range, oxide capacitance is main factor that determine the electrical property. In the mid frequency range from 0.1GHz to 2GHz, silicon substrate capacitance is dominant factor that determine the level of insertion loss. Lastly, over 2GHz frequency range, insertion loss rapidly increases due to the inductance of TSV. According to different frequency range, electrical characteristic of TSV is different. Whereas, electrical property of glass channel mainly affected by the inductance of vias. In the overall frequency range, insertion loss is determined by combination of inductance of via and capacitance of glass substrate. Insertion loss of TGV channel increased slightly due to dielectric loss.

Glass channel shows significant insertion loss because of impedance mismatch at through glass via. S21 magnitude fluctuates with certain period. This large ripple is occurred by reflection wave due to impedance mismatch at TGV. In the silicon interposer, reflected wave occurred by impedance mismatch at TSV pass thorough conductive silicon substrate. Therefore, effect of impedance mismatch is not that large in the TSV channel. On the other hand, due to high resistivity of glass substrate, reflected wave cannot pass through glass substrate. The period of fluctuation is constant value which is determined by material property and overall channel length. Because multiple via transition channel has 8 times longer length than single via transition pattern, first peak frequency of impedance mismatch is lowered to 5GHz. As shown in figure 3, single via transition channel has first peak around 25GHz.



(a)



(b)

Figure 6. Eye diagram simulation result of single-ended (a)TSV channel, (b)TGV channel at the data rate of 3.2Gbps.

The simulated eye-diagrams of silicon and glass channel at the data rate of 3.2Gbps are shown in figure 6(a) and (b). In the multiple via transition silicon channel, we can find significant eye-diagram distortion by inter-symbol interference. Eye height of silicon channel is 58.8% of peak-to-peak voltage. Whereas, eye height of glass channel is 96.6% of peak-to-peak voltage. At the data rate of 3.2Gbps, frequency range under 8GHz mainly affect the eye-diagram result. Because the glass channel rarely shows insertion loss in this range, eye diagram of glass channel is better than that of silicon channel.

In the time domain simulation, rising and falling time of input signal increase according to RC delay of channel. Due to larger capacitance of silicon channel, it shows longer rising and falling time as shown in figure 6. In the glass channel, rising and falling time is short due to small value of glass substrate capacitance compared to large oxide capacitance and silicon substrate capacitance. Because of reflection from impedance mismatch at TGV, voltage increase as step curve. Timing jitter of silicon channel also has quite large value as 18.69% of one unit-interval (UI). On the other hand, glass channel shows 0.3ps timing jitter which is 0.05% of 1UI.

C. Analysis of Impedance Mismatch at Via Pad

In the previous part, we simulated TSV and TGV channels whose line width and via pad diameter are the same. In this part, we intentionally changed proportion of line width and via pad diameter to observe the impedance mismatch effect at via pad. S21 magnitude of silicon channel slightly increases over 2GHz frequency range due to impedance mismatch. On the contrary, TGV channel has large drop due to impedance mismatch between TGV and line. Insertion loss at the frequency of first drop is 3.73dB, 0.91dB respectively when the line width is 16μm and 160μm. Especially, at the frequency of first drop of glass channel, the insertion loss is as large as that of silicon channel. Therefore, we should carefully design TGV channel considering characteristic impedance difference between line and TGV.

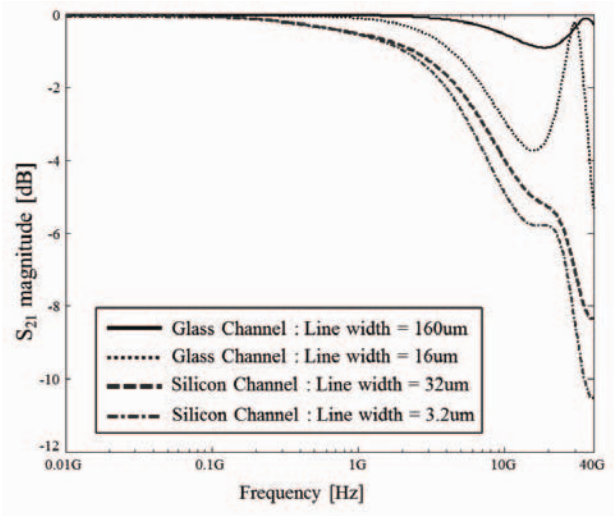


Figure 7. The dimension of TSV and TGV channel for time-domain and frequency-domain simulation

IV. CONCLUSION

In this paper, we compared the electrical characteristics of TSV and TGV. We simulated TSV and TGV channel with single and multiple via transition. Structural dimension and stack-up are based on the minimum fabrication design rule. We designed the channel considering more fine pitch fabrication of silicon interposer. We analyzed the time-domain and frequency-domain simulation results. Insertion loss (S21) level of silicon channel is significantly lower than that of glass interposer. Because of conductivity of silicon substrate, the loss of silicon channel is more significant. We also verified this tendency with eye-diagram simulation. Electrical characteristic of TSV is determined with oxide capacitance, silicon substrate capacitance and inductance of via. On the other hand, due to absence of insulation layer, inductance of via is most dominant factor of TGV. We verified these properties using TDR simulation result of TSV and TGV channel. As frequency increases, loss of TSV channel significantly increases. Meanwhile, dielectric loss of TGV channel is not that large. However, the effect of impedance mismatch at TGV degrades the signal integrity at certain frequency. We should carefully design TGV channel because it is more sensitive to impedance mismatch.

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