# Precise RLGC Modeling and Analysis of Through Glass Via (TGV) for 2.5D/3D IC

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**Abstract**

Through glass via (TGV) is most important technology in the glass interposer. Electrical characteristic of TGV determines the overall signal integrity of signal paths in 2.5D/3D system. It is essential to electrically model TGVs for analysis of overall 2.5D/3D IC system including digital or analog chip. In this paper, we proposed the precise RLGC circuit model of single-ended signal TGV. Each equation of RLGC is a function of design parameters such as height, diameter of through glass via and pitch between GS pair, and material properties such as permittivity of glass and polymer. Proposed model is verified up to 40GHz with full-3D simulation. Using the proposed model with parasitic components of through glass via, we analyzed the electrical characteristic of TGV in frequency and time domain.

**Introduction**

3D-Integration has become a key solution to overcome technical challenges associated with the performance saturation and limitation of CMOS technologies. With shorter interconnection length and shorter electrical delay, 3D integration technology provides significant performance improvement in the high-speed and high-bandwidth system. To increase I/O density, however, organic substrate is the bottleneck of the high-density packaging. The concept of interposer is introduced as interconnecting medium to remove dimension gap between very fine-pitch chip and loose-pitch printed circuit board. The interposer leads to achieve high-bandwidth because of small pitch and wide I/O.

Currently, silicon is the material most often used in interposer fabrication. However silicon interposers show significant signal loss at the high frequency and high cost limits. Whereas glass has very low insertion loss because of its high electrical resistivity. Glass as an interposer material have advantages not only intrinsic electrical property but also better feasibility with low CTE mismatch and most importantly large size availability. Also, manufacturing cost of glass is much lower than silicon process which is on-chip metal process. Massive production of glass interposer is possible since it is processed from large panel fabrication. These are why using glass for the interposer substrates can be a superior alternative to address the limitations of silicon interposer. [1][2]

This paper focused on a high-frequency scalable electrical modeling of Through Glass Via (TGV) which is the core technology in the glass interposer. There have been several publication focusing on the electrical model of Through Silicon Via (TSV) [3][4]. However, an accurate circuit model of TGV has not yet been proposed. Although the physical dimension of TSV and TGV is similar, the electrical characteristic of TGV is distinct from TSV. Semiconductor properties of the silicon substrate and capacitance between silicon substrate and oxide are dominant factor in modeling TSV. TGV however, due to high resistivity of glass substrate, effect from inductance and resistance of via is significant. Accurate electrical model of TGV considering glass fabrication and electrical characteristic of glass substrate is proposed to estimate overall electrical performance combining with other circuits. Proposed model of TGV considering the physical configuration is verified by 3D full wave electromagnetic (EM) simulation. The value of RLGC parameter of TGV are summarized in the table with the dimension of glass interposer fabrication design rule determined by Packaging Research Center, Georgia Institute of Technology. Based on proposed TGV model, the high-frequency electrical behavior and signaling performance is analyzed in the time domain and frequency domain. We analyzed loss mechanism of TGV using characteristic impedance and s-parameter of proposed model.

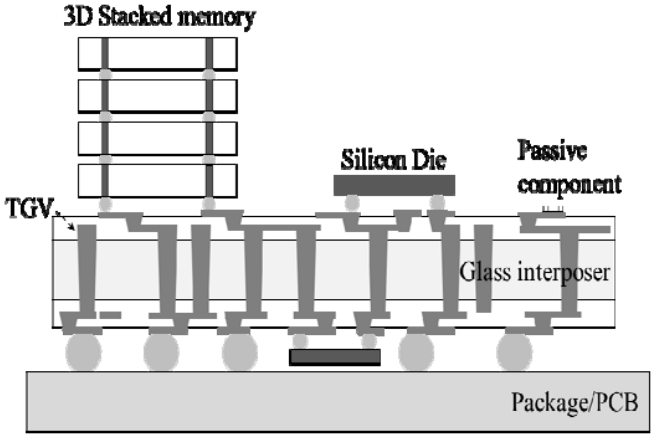



**Figure 1.** The concept of 3D IC with glass interposer, which includes 3D stacked memory and silicon logic die on both top and bottom of glass interposer.

**Proposal of the equivalent circuit model of a TGV**

Figure 2 shows glass interposer and TGV structures. There are structural parameters that is determined by glass interposer fabrication design rule. Therefore, proposed equivalent circuit model can fully express the physical meaning of each structural parameter with simple equation. Basically, all the parameters derived from the model of coaxial cable. Even though, the actual structure of TGV is observed to be tapered,

the electrical characteristic of tapered via is almost same as cylindrical via. It shows slight difference in s-parameter over target frequency of proposed model. The Top pad and bottom pad for TGV have same dimension. Equation for each parameter summarized as follows.

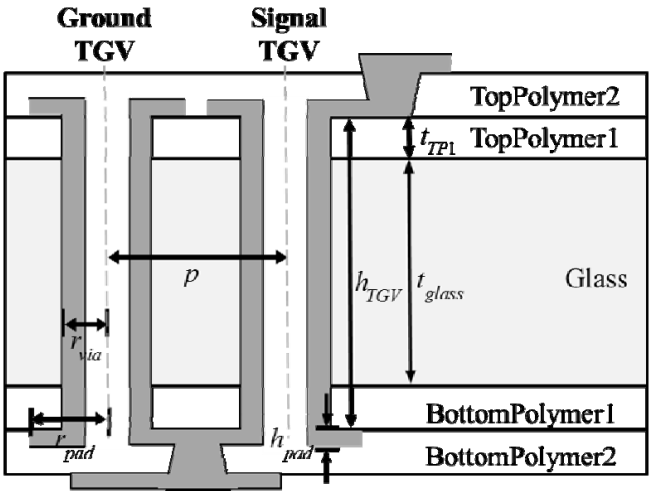



**Figure 2.** The dimension of glass interposer for modeling and simulation .

TABLE 1
Model parameters with their symbols for a proposed scalable electrical model of TGV

| Parameter | Description | Value |
|---|---|---|
| $r_{via}$ | Radius of via | 50um |
| $r_{pad}$ | Radius of pad of TGV | 80um |
| $p$ | Pitch between signal and ground TGVs | 300um |
| $h_{TGV}$ | Height of via | 135um |
| $h_{pad}$ | Height of pad of TGV | 10um |
| $\varepsilon_{glass}$ | Relative permittivity of glass substrate | 5.3 |
| $\varepsilon_{polymer}$ | Relative permittivity of polymer substrate | 3 |
| $\tan\lvert\delta d\rvert_{glass}$ | Loss tangent of glass substrate | 0.004 |
| $\tan\lvert\delta d\rvert_{poly}$ | Loss tangent of polymer substrate | 0.005 |
| $t_{glass}$ | Thickness of glass substrate | 100um |
| $t_{BP1}$ | Thickness of bottom polymer1 | 17.5um |
| $t_{TP1}$ | Thickness of top polymer1 | 17.5um |

$$R_{TGV} = \sqrt{(R_{ac}^2 + R_{dc}^2)}[\Omega] \quad (1.a)$$

$$R_{ac,via} = \frac{p}{2\times r_{via}} \times \rho_{copper} \times \frac{h_{TGV}}{\pi\times(2\times R_{via}\times\delta_{skin} - \delta_{skin}^2)} \quad (1.b)$$

$$R_{dc,via} = \rho_{copper} \times \frac{h_{TGV}}{\pi \times r_{via}^2} \quad (1.c)$$

$$\delta_{skin} = \frac{1}{\sqrt{\pi f \mu \sigma}} \quad (1.d)$$

Resistance of TGV is a function of pitch between signal and ground TGV, height and diameter of TGV. Also, the resistance is frequency dependent because of skin effect as frequency increases. It is separated into two part, $R_{ac,via}$ and $R_{dc,via}$, which includes the skin effect term or not. [5][6]

$$L_{TGV} = \frac{1}{2}\times\frac{\mu_{copper}}{2\pi}\times h_{TGV}\times\ln(\frac{p}{r_{via}})[H] \quad (2.a)$$

$$L_{pad} = \frac{1}{2}\times\frac{\mu_{copper}}{2\pi}\times h_{pad}\times\ln(\frac{p}{r_{pad}})[H] \quad (2.b)$$

Because TGV capacitance is usually much smaller than that of TSV, capacitance has only limited effects on electrical characteristics of TGV. On the other hands, the inductance greatly affects the electrical characteristics. Inductance increases as height and pitch of TGV pair increase, and diameter of TGV decreases. Inductance equation is calculated considering both self and mutual inductance. Both inductances for via and pad can be derived from the loop inductance model between two parallel conducting wires. [7]

$$C_{polymer,pad} = \frac{\varepsilon_{polymer}\times\varepsilon_0\times\pi\times h_{pad}}{\ln(\frac{p}{r_{via}})}[F] \quad (3)$$

$$\sigma_{polymer} = \tan\lvert\delta d\rvert_{poly}\times 2\pi f\times\varepsilon_{polymer} \quad (4.a)$$

$$G_{polymer,pad} = \frac{\sigma_{polymer}}{\varepsilon_{polymer}} C_{polymer,pad}[S] \quad (4.b)$$

There are capacitance and conductance between ground and signal TGV pads filled with glass substrate. Capacitance can be derived from parallel wires capacitance equation. It is a function of height, pitch between GS pairs and diameter of TGVs. Glass interposer material property, which means the relative permittivity of glass and polymer also affects the value of capacitance. The conductance of glass substrate had reliably low value. The equation for conductance of glass is determined by the relationship with capacitance.

Because there is a dielectric mixture composed of glass and polymer between GS TGVs pair, we used effective dielectric permittivity to calculate the capacitance and conductance of multilayer. Equation for calculation of effective dielectric permittivity is as follows. It is determined as a function of thickness of each layer and intrinsic electrical properties. Also, in the same way, we can calculate the conductivity of mixed layer of polymer and glass.

$$\varepsilon_{eff} = \frac{h_{TGV}}{\frac{t_{glass}}{\varepsilon_{glass}} + \frac{t_{BP1}}{\varepsilon_{polymer}} + \frac{t_{TP1}}{\varepsilon_{polymer}}} \quad (5)$$

$$C_{glass+polymer,TGV} = \frac{\varepsilon_{eff} \times \varepsilon_0 \times \pi \times h_{TGV}}{\ln(\frac{p}{r_{via}})}[F] \quad (6)$$

$$G_{glass+polymer,TGV} = \frac{\sigma_{glass+polymer}}{\varepsilon_{glass}} C_{glass+polymer,TGV}[S] \quad (7)$$

We used single stage lumped model with RLGC equation as shown in figure 4. Lumped approximation is valid because the height of TGV is small enough compared to the wavelength of maximum target frequency. At 40GHz frequency, the wave length is 3.25mm at the effective dielectric constant of glass which is 5.3. The height of TGV is 135um which is smaller than wavelength over 20.

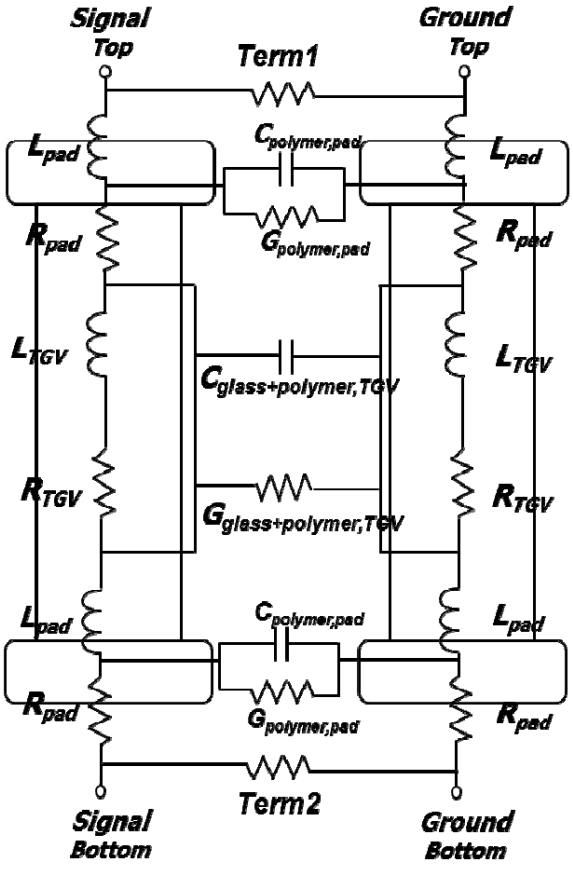



**Figure 3.** Proposed electrical circuit model with RLGC components.

**Model verification with frequency-domain simulation**

To verify the proposed circuit model of single-ended GS TGV pairs, S-parameter from the proposed model and Ansys HFSS simulation are compared. In the HFSS simulation, we used lumped port to excite structure and calculated impedance matrices and s-parameters. Lumped port can be neglected when path go through lossy material because the value of port inductance is relatively very small. But in this case, due to small height of via under 150um and low signal loss through glass substrate, port inductance cannot be neglected. We inserted inductance next to the terminal in the circuit simulation setup to consider effect from lumped port in the 3D simulation.

Figure 4 shows the magnitude and phase of insertions loss and return loss for both modeled and simulated TGV pair. As you can see in figure 4, there is close correlation up to 40GHz between two graphs from circuit model and simulation. There is a small mismatch of phase of return loss in the low frequency range. This is because of assumption of resistance in the equation (1.a). However this error is allowable because it is smaller than 0.01%. From these result, we can see that the parameters for TGV model is well-defined. We observed the change of s-parameter as we change each value of RLGC. The dominant factor that decided the abstract shape of s-parameter graph is inductance of via and pad and capacitance between GS pairs. The resistance highly affects $S_{11}$ phase under 1GHz. Due to high resistivity of glass, the s-parameter rarely changed with variation of conductance. Table 2 shows the calculated value of RLGC parameter used in proposed circuit model at 40GHz. All the parameters such as height, pitch and Rvia are given in the table1.

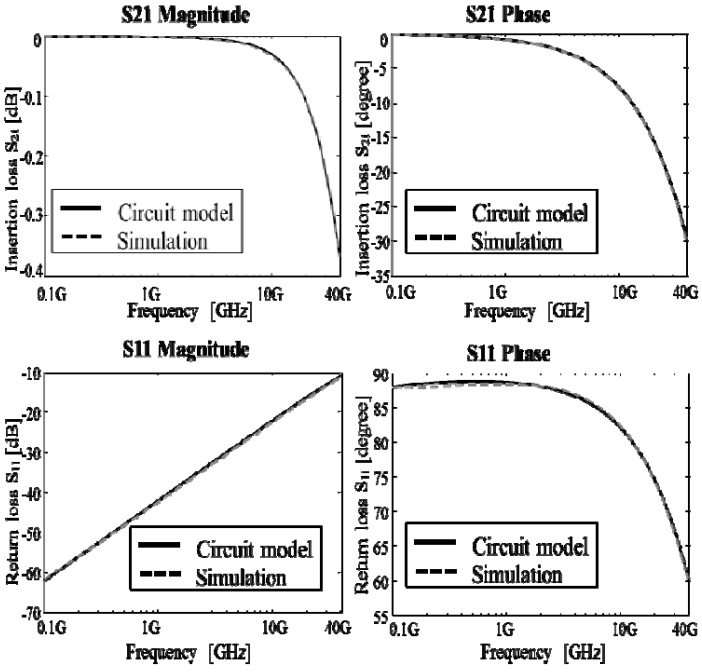



**Figure 4.** Model verification with comparison of magnitude and phase of insertion loss and return loss from proposed circuit model and full 3-D simulation

TABLE 2
The value of RLGC parameter for through glass via and pad at the 40GHz

| $R_{TGV}$ | $L_{TGV}$ | $G_{TGV}$ | $C_{TGV}$ |
|---|---|---|---|
| 2 $m\Omega$ | 24.1 $pH$ | 7.24 $nS$ | 15.1 $fF$ |
| $R_{pad}$ | $L_{pad}$ | $G_{pad}$ | $C_{pad}$ |
| 72.1 $\mu\Omega$ | 1.32 $pH$ $pH$ | 65.9 $nS$ | 1.3 $fF$ |

**Analysis of electrical characteristics of TGVs**

Characteristic impedance graph of single-ended signal TGV with variation of pitch between GS pair is shown in figure 5. As pitch between GS pair increases, the peak value of impedance increases. With dimension of glass interposer shown in figure2, the impedance of single-ended signal TGV is 51.39 $\Omega$ with the 300um pitch. It increase up to 54.99 $\Omega$ with 600um pitch between GS pair. Inductance and resistance of via increase with increase of pitch. In contrast, capacitance and conductance of glass substrate decrease as pitch between GS pair increase. As a result, increase of resistance and inductance and decrease of capacitance and conductance of TGV results in increased impedance given by the Equation 6.

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (8)$$

In the RF system where 50 Ohm matching is required for signal path, we can minimize the loss from impedance mismatch by decreasing TGV pitch. However, because of process limitation, it is not easy to succeed in the reduction of pitch between TGV under 300 um. In that case, inserting ground TGV near the signal TGV could increase capacitance and therefore decrease characteristic impedance to match the impedance to 50 Ohm. Also, to minimize the mismatch in the glass via, we can insert more than one ground via near the signal via.

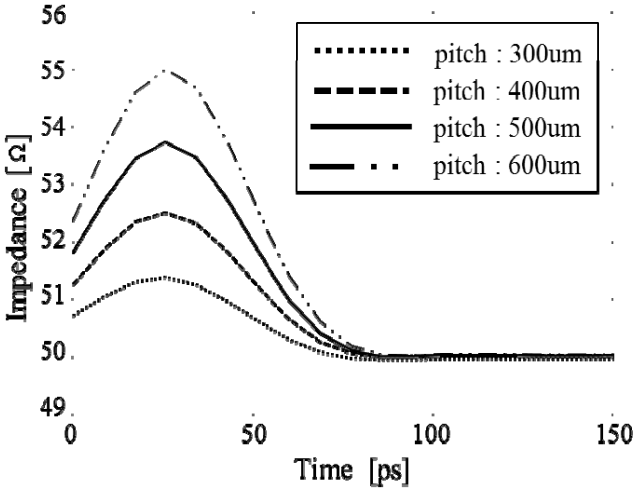
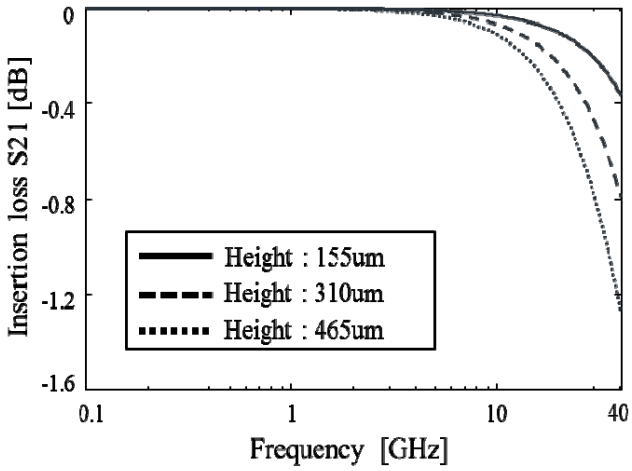
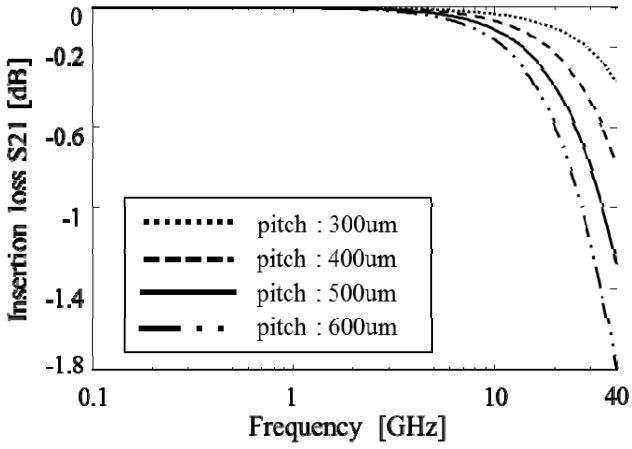


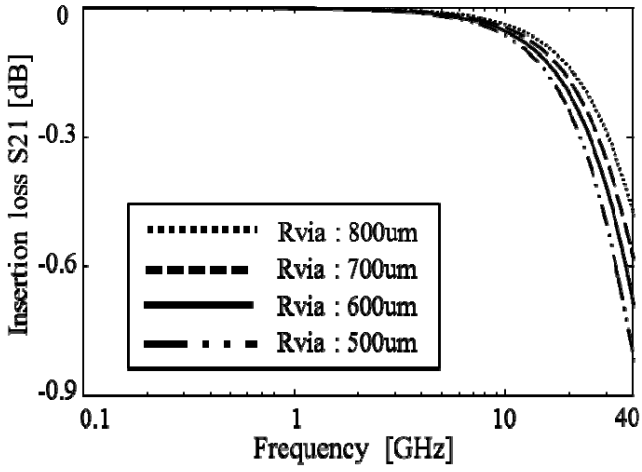

**Figure 5.** Time-domain simulation result of single-ended TGV with variation of the pitch between GS pair




(a)




(b)




(c)

**Figure 6.** Frequency-domain simulation result of single-ended TGV with variation of the (a) height (b) pitch between GS pair (c) diameter of TGV

Figure 6 shows the frequency domain simulation result of single-ended TGV from 0.1 GHz to 40 GHz with the variation of height, pitch between GS pairs and diameter of TGV.

First, we observed the variation of s-parameter graph as we change the thickness of glass and polymer layer and height of TGV two times and three times of original value. This can be considered as repetitive 2 or 3 stages of single lumped circuit we proposed. Inductance, resistance, capacitance and conductance increased all together with the rate of height of TGV. The impedance of TGV increase as the resistance and inductance increase. Meanwhile, the impedance of TGV decrease as the conductance and capacitance increase. In figure 6 (a), as height of TGV increase, we can find that the insertion loss decrease in the high frequency range above 5Hz. Even though the capacitance increases as height increase, the insertion loss decreased because of effect of inductance of TGV in the high frequency region. This means that the inductances of via and pad have more effect than capacitances to insertion loss.

Figure 6(b) showed the insertion loss graph with variation of the pitch between GS pair. As discussed, the inductance of TGV increased up to 33.5 pH from 24.1 pH and the capacitance of TGV decrease until 9.26 pF from 15.1 pF as the pitch increase from 300 um to 600 um. These change results in the decrease of insertion loss. When the pitch between GS pair is 600um, the insertion loss decrease to -1.79dB at 40 GHz. Compared to other dimension parameter, the pitch between GS TGVs has greatly decrease insertion loss as it increase. But in this result, the effect from port inductance is included. Meanwhile the port inductance is fixed when the height and diameter of TGV changed, the port inductance increase with the rate of pitch. Because port inductance is significant number compare to inductances of TGV and pads, this results in significant increase of insertion loss.

Diameter of TGV is also parameter that affects the magnitude of insertion loss. When diameter of TGV increased, the inductance decrease and capacitance increase on a logarithmic scale. In the case of 500 um diameter, the inductance of TGV is 24.1 pH. As diameter increases, inductance of via decreases until 17.8pH. Meanwhile, the capacitance increase from 15.1 pF to 26.4 pF, as diameter increase from 500 um to 800 um. Due to small variation of value of inductance, there is a relatively small decrease in insertion loss. With dimension of glass interposer proposed in figure 2(a) and table 1, insertion loss is 0.47 dB at 40 GHz. It increase up to -0.80 dB with 500 um diameter.

With the result of frequency-domain simulation, we observed the change of insertion loss as the dimension of TGV is changed. Insertion loss decreases when the height and pitch between GS pair decrease and the diameter of through glass via increase. Also, in the high frequency range, insertion loss decrease when the value of inductance decrease and the value of capacitance increase. Due to high electrical resistivity of glass substrate, the effect from conductance of glass and polymer layer was rarely expressed. Increase of resistance of via and pad decrease insertion loss in the overall frequency range.

**Conclusions**

Due to demands for highly dense packaging and higher system performance, glass interposer becomes one of the solution to satisfy both of them. As an interconnection of glass interposer, through glass via (TGV) is a core technology due to its small loss. In this paper, analytic model of TGV is proposed. The proposed model fully express the physical meaning of each structure parameter such as height, pitch between GS pair and diameter of via. We showed that the proposed equivalent circuit model is well correlated with result of full 3-D simulation. The exact value of resistance, inductance, capacitance and conductance are summarized for single-ended GS pair of TGVs.

With time domain simulation, characteristic impedance of TGV is derived. Also, we analyzed the dominant factors which affect the frequency dependency of loss with variation of structural parameter. Inductance of via is most dominant parameter to the result of s-parameter. From the result of frequency domain simulation, we confirmed that the insertion loss of TGV is minimized with minimum height and pitch between GS pair and maximum diameter of through glass via.

In this paper, we use assumption of cylindrical via of copper. However, the actual structure of TGV is observed to be tapered. From the simulation result, tapered via has more loss than cylindrical via. Even though the value of s-parameter is not significantly different from cylindrical assumption, to obtain more accurate via model, it is worth to modify the model of TGV with tapered shape via.

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**References**

1. Vijay Sukumaran, Tapobrata Bandyopadhyay, Venky Sundaram, Rao Tummala, "Low-Cost Thin Glass Interposers as a Superior Alternative to Silicon and Organic Interposers for Packaging of 3-D ICs," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol.2, no.9, pp.1426,1433, Sept. 2012
2. Vijay Sukumaran, Qiao Chen, Fuhan Liu, Nitesh umbhat, Tapobrata Bandyopadhyay, Hunter Chan, Sunghwan Min, Christian Nopper*, Venky Sundaram, and Rao Tummala. "Through-Package-Via Formation and Metallization of Glass Interposers" *IEEE Electronic Components and Technol. Conf. (ECTC),* Las Vegas, NV, USA, 1-4 June 2010, pp. 557 - 563
3. L. Cadix, A. Farcy, C. Bermond, C. Fuchs, P. Leduc, M. Rousseau, M. Assous, A. Valentian, J. Roullard, E. Eid, N. Sillon, B. Flechet, and P. Ancey, "Modelling of through silicon via RF performance and impact on signal

transmission in 3-D integrated circuits," in Proc. *IEEE 3-D Syst. Integration Conf,* San Francisco, CA, Sep. 28–30, 2009, pp. 1–7.
4. Joohee Kim, Jun So Pak, Jonghyun Cho, Eakhwan Song, Jeonghyeon Cho, Heegon Kim, Taigon Song, Junho Lee, Hyungdong Lee, Kunwoo Park, Seungtaek Yang, Min-Suk Suh, Kwang-Yoo Byun, Joungho Kim , "High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)," *Components, Packaging and Manufacturing Technology, IEEE Transactions on* , vol.1, no.2, pp.181-195, Feb. 2011
5. S. H. Hall, *High Speed digital System Design*. New York: Wiley.
6. F. Terman, *Radio Engineer's Handbook*. New York: McGraw-Hill, 1943, p. 43.
7. M. N. O. Sadiku, *Elements of Electromagnetics*, 3rd ed. New York: Oxford Univ. Press.