Fabrication and Integration of Ultrathin, High-Density, High-Frequency Ta Capacitors on Silicon for Power Modules

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Abstract— This paper demonstrates silicon-integrated, thinfilm, high-density tantalum capacitors for integrated power modules. The capacitors in form-factors of less than 75μm showed stable capacitance densities of more than 0.3 $\mu F/mm^2$ with leakage of less than 0.1 $\mu A/\mu F$ at 3 V. To the best of authors' knowledge, this is the highest capacitance density reported till date at the mentioned form-factors. Furthermore, these capacitors are integrated directly above the active silicon, enabling shorter interconnection path with lower system parasitics, leading to higher switching frequencies and lower losses. These ultra-miniaturized, substrate-compatible tantalum capacitors, thus, address the strategic need for highly-efficient, ultra-miniaturized power modules.

Keywords-silicon; capacitance density; power modules; integration

I. INTRODUCTION

Power supplies with minimum noise levels are required for high performance and efficiency. Passive components such as decoupling capacitors help achieve these noise levels by bypassing high impedance power supply components in the circuit. The traditional discrete capacitors that are board-mounted are limited due to their long interconnection lengths that induces large parasitic inductances and limit their operating frequency. However, if the decoupling capacitors are placed close to the active IC, they can be far more effective with reduced inductances from shorter interconnection lengths [1]. Glass- and silicon- based interposer technologies that utilize vertical through-via interconnections have shown way to improve power distribution network (PDN) performance with thin power-ground planes [2-4]. However, integration of ultra-high density capacitors in such substrates has not yet been demonstrated. Integration of decoupling capacitors in multichip power modules close to active chip has, therefore, been researched extensively.

Two approaches have been pursued to improve the effectiveness of capacitors by placing them close to the ICs: trench capacitors and embedded capacitors. Trench capacitors are used in on-chip regulators. The on-chip regulators mitigate the interconnection parasitic issues due to ultrashort distance to the loads compared to off-chip voltage regulators [5], thus, providing faster response and improved power delivery networks. However, they are limited to low voltage and current rating with degraded convertor efficiency, increased process complexity and die cost. The limited aspect ratios also pose a challenge in terms of achieving higher capacitance density. In addition, the use of expensive tools renders them non-scalable for high-volume manufacturing so as to end up with low cost. Similarly, the fully-integrated-voltage-regulator [6, 7] by Intel with their Haswell processors eliminates several external power management ICs, with MIM capacitor on die or trench capacitors. The efficiency of these switching regulator also gets strongly affected by the capacitors since these regulators draw high peak currents from the capacitors when switched on. The regulator is known to operate most efficiently when there are minimum switching losses, which in turn requires high-frequency capacitors with low impedance. The designed high-frequency switching capacitors thus need to be placed closest to the switch FET to keep the trace inductance to a minimum. Leading-edge, discrete but thin capacitors such as multilayered ceramic capacitors (MLCCs), owing to their thin form-factors with high density provides the capability to be integrated close to the IC. MLCCs from Murata that are less than 150 μm thick, are embedded in thin organic laminates or assembled on the backside of the package [8] to reduce the inductance and provide more efficient power convertors.

Embedded thinfilm decoupling capacitors rely on thin high-permittivity dielectrics to be able to integrate close to IC. These include ferroelectrics such as barium titanate and lead lanthanum zirconate titanate [9-12]. In addition to the high processing temperatures (>700ºC) of the above-mentioned ferroelectrics, they also show poor voltage response that limits their applications in power electronics. Several groups have also worked on tantalum pentoxide dielectrics (Ta_2O_5) for planar [13, 14] or TSV- or TPV-

integrated [1, 15] decoupling capacitors. However, Ta_2O_5 thin-film capacitors are limited to low capacitance densities (~5 nF/mm^2) that would require large-area capacitors to meet the required capacitance. High-density capacitors, on the other hand, occupy large volumes and are placed far away from the chips owing to their packaging which degrades their performance at higher operating frequencies. Some of these large surface-area capacitors include multilayered co-fired ceramic capacitors, etched foil capacitors and discrete tantalum capacitors [16-18]. Although MLCCs combine small size, low ESR, low ESL, and wide operating temperature range, they show large and dramatic variation with temperature, dc bias, and ac signal level. On the other hand, solid tantalum capacitors are less sensitive to temperature, bias and variation as compared to MLCCs. Particulate-electrodes such as tantalum-based capacitors also suffer from large conduction pathways of the electrode increasing the ESR of the electrodes leading [19-21] to higher time constants according to the equation (1).

$$\omega\tau = 1 \qquad (1)$$

Here, ω = operating (angular) frequency, and τ = time constant which is a product of ESR and the capacitance. Particulate-based electrodes can also suffer from insufficient cathode coverage inside the porous structure leading to high ESR and ESL values that adversely affect their operating frequencies.

Thin particulate electrode-based tantalum capacitors with high surface area per unit volume, if integrated directly on silicon, can meet the capacitance targets at operating frequencies beyond 1MHz for decoupling, without taking up extra package space. The unique combination of thinner porous network on metal foil, along with conducting polymer cathodes and direct metallization can act as a solution to high ESR values in the studied capacitor structures.

The key process challenge with current tantalum capacitors is the high processing temperature for electrode formation. This paper demonstrates an innovative approach to address this challenge by prefabricating the electrodes on a free-standing foil, which are then transferred onto the active wafer to form the capacitors on Si. The integration approach is designed to also embed these thin tantalum capacitors on alternative substrates such as organic, glass or silicon, with copper via interconnections for lower parasitics. A schematic of the integrated capacitor structure with electrodes, dielectrics and copper via interconnections is shown in Fig. 1.
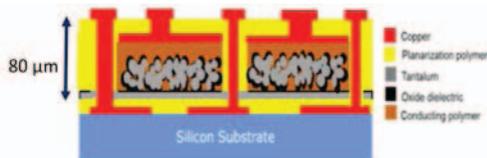

Figure 1.   Cross-section of high-density thin tantalum capacitors on silicon.

II. EXPERIMENTAL

Integration of tantalum capacitors on silicon as thin-films is described in two parts; the first part (A) describes the fabrication of tantalum capacitors on active silicon wafers. This is accomplished by sintering sub-micron tantalum particles on free-standing 25 micron tantalum foil at relatively high temperatures to form a porous tantalum anode, which is then laminated onto silicon. The anodes were prepared and provided by H.C. Starck by stencil printing technology. A thin 25 µm Ta foil was used as a substrate and Ta paste was applied via a stencil on it. The samples were debindered and sintered at temperatures > 1000°C to have an adequate binding from substrate to Ta powder. The foil was then laminated onto the active wafer using an adhesive (ABF® dielectric) at 200 ºF and high pressure (1 MPa). This is followed by anodization and counter electrode deposition to form the capacitor structure. The second part (B), describes the integration steps such as passivation, planarization, via-formation, metallization etc. to form the build-up layers.

A. Tantalum Capacitor Fabrication

The free-standing tantalum foil with porous anodes was laminated onto silicon using an epoxy adhesive (ABF®). Extra caution was taken during the adhesive lamination to ensure no copper pads that formed metal terminal traces on silicon remain exposed. This is required to prevent any copper leaching into the electrolytic bath during anodization. Copper ions from electrolytic bath are known to get trapped in the oxide dielectric, yielding poor quality dielectric. Anodization of the tantalum foil on silicon was carried using conditions outlined in Table. I.

TABLE I.   ANODIZATION CONDITIONS

Parameters	Values
Electrolyte	Phosphoric acid
Electrolyte concentration	0.1 M
Voltage	20V
Temperature	Room temperature

The cross-section of tantalum anode and tantalum oxide is shown in Fig. 2(a) and (b) respectively. The cathode application was carried out using a dip-coating method. Conducting polymer suspension, PEDT:PSS in water, served as a self-healing, counter electrode when infiltrated into the nanoporous channels of the anode. The polymer coverage in the nanochannels plays an important role and determines the capacitance and ESR for a capacitor. Conformal and thick coverage was achieved (Fig. 3(a)) by multiple dippings in several concentrations of the polymer. The conducting polymer was later selectively patterned using plasma RIE (reactive ion etching) where the sputtered gold on capacitor pads (Fig. 3(b)) acted as metal mask. Zeiss Ultra60 FE-SEM was used for the morphological analysis. HP 4285A precision LCR meter was used for C-V and frequency stability measurements. Keithley 6485 picoammeter was used for the leakage current analysis.
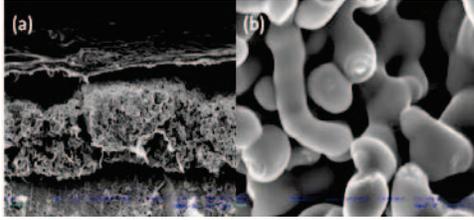
Figure 2.   Cross-sectional SEM of (a) tantalum anode; (b) anodized tantalum anode with 50 nm Ta$_2$O$_5$ shell on metal core.
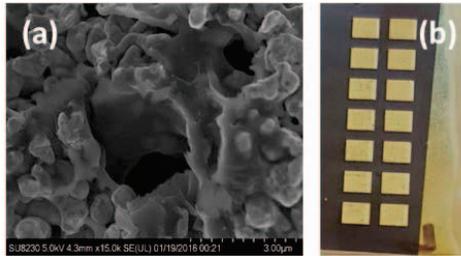

Figure 3.   (a) Cross-section SEM image of conducting polymer infiltrated into the tantalum electrode structure; and (b) picture of fabricated capacitor array on tantalum foil.

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B. Silicon-integration of Thin-film Tantalum Capacitor

The integration scheme is designed to be compatible with large-area active silicon and high-through-put glass interposers and packages. Low-cost and large-area panel-compatible processes are utilized. The detailed process-flow of thin-film tantalum capacitors is shown in Fig. 4.

III.   RESULTS AND DISCUSSION

Upon completion of capacitor fabrication, the capacitor array is first passivated using a polymer coat to prevent any moisture and oxygen penetration in the capacitor structure. Conducting polymer is known to be water-and oxygen-sensitive that can show pseudo-capacitance if left unprotected. During high-temperature operation for long durations, moisture trapped in the organic cathode can start creating ion deficiencies leading to capacitor failures. For

this study, 25 nm of paralyene was deposited using CVD on the tantalum capacitor array. This low-temperature deposition leads to highly-conformal passivation layer with uniform thickness of 25 nm. Thicker paralyene is generally not recommended due to its high stiffness that can induce stresses in the film leading to delamination.

The prerequisite material properties for planarization polymer are 1) easy flowability during hot-pressing for planarization 2) high toughness: high elongation to failure; 3) low loss; 4) low moisture uptake; 4) low temperature of curing; and 5) commercially available in different thicknesses.

Polyimides have very high elongation to failure and are widely used as RDL dielectric in wafer level packaging. However, they have high temperature of curing (ca. 300ºC) and high moisture absorption of 1.5%. Other polymers such as BCB (benzocyclobutene), siloxane and photo-definable polymers were also evaluated for passivation. However, most of the polymers showed low toughness and high temperature of curing. A key feature of planarization polymer is its easy flowability under hot-pressing to ensure planarity and complete filling. Epoxy with silica fillers (ABF®) was thus chosen as the layer due to its easy flowability at high temperature and pressure, low loss and availability. ABF epoxy was laminated and cured to form the planarization layer as shown in Fig. 5. The polymer dielectric in conjunction with paralyene can act as an effective passivation and planarization layer with low moisture uptake, low loss and low curing temperature.
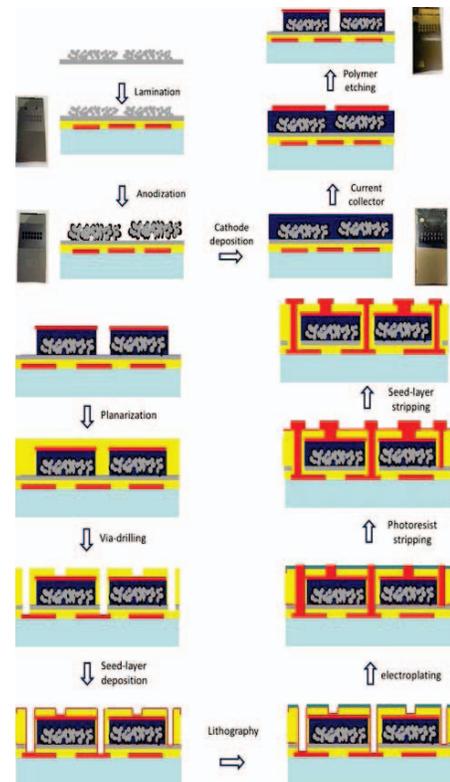

Figure 4.   Process flow for integration of high-density Ta capacitors on silicon.

To access the bottom (Ta anode) and top (polymer and gold) electrodes, vias were drilled through the passivation and planarization layers. CO_2 laser was used to drill through the silica-filled polymer while ensuring no damage was done to the underlying metal electrodes. Extra caution during drilling was entailed due to the thickness variation in the planarization polymer, ~15 µm on the gold pad and ~35 µm on tantalum foil.

The diameter of drilled vias was measured to be ~300 µm on the top and ~200 µm on the bottom with a taper of 45° for via on tantalum electrode (Fig. 6c). CO_2 laser has a high ablation rate on polymer while very low rate on metals, thus selectively removing the polymer alone. The roughness of via bottom on gold electrode was several order of magnitude higher than the via on tantalum, as can be seen in Fig. 6(a,b). The roughness on gold is attributed to the underlying tantalum topography that originates from stencil printing of tantalum. Laser ablation of polymer generally leaves organic and silica residues behind, which is cleaned using dry etch RIE (reaction ion etching) process with CHF_3 and O_2 gas precursors.

Drilled vias were finally electroplated to form all-copper interconnections. Low electrical resistivity, high electromigration resistance, simple and cost effective deposition techniques make copper a primary candidate for interconnection material. Electroplated copper provides void-free fill with low resistivity, and large grain size of copper, which is responsible for its high electromigration

resistance and higher reliability [22]. Electroplating bath consisted of cupric ions, sulfuric acid and trace organic additives. Electrical contact was made to the seed layer and current was passed to reduce the copper ions on the surface of the sample. The additives consisted of suppressors such as polyethylene glycol that reduces the plating rate at the top of the vias by blocking of growth sites on the copper surface. Other additives such as dimercaptopropane sulfonic acid accelerates plating in the bottom of the vias [22]. The conditions of the electroplating are mentioned in Table II. The optical image of partially-filled copper vias is shown in Fig. 7(a,b) while top view image of completed integrated thin-film, tantalum capacitor array is shown in Fig. 7(c).

Electrical Characterization

The capacitance density of the thin tantalum capacitors was measured to be 0.3 µF/mm² at 100 kHz with 0V bias and 100 mV peak amplitude. Fig. 8(a) illustrates the capacitance density vs frequency plots for the free-standing tantalum capacitor array.

The initial curve of capacitance, without any parasitic correction (gray curve in Fig. 8(a)) shows the capacitor resonance frequency at 1 MHz, which is attributed to the parasitic ESL from the tool cables. The measurements were then made after correcting for cable inductance (tool parasitics) and pad inductance (using same sized parallel plate capacitor). The capacitors showed stable capacitance density of 0.3 µF/mm² till 1.2 MHz, before showing capacitance roll-off.
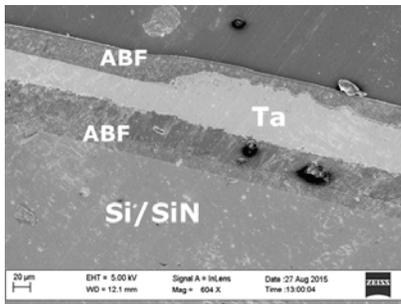

Figure 5.   SEM micrograph of laminated tantalum capacitor foil on silicon substrates.
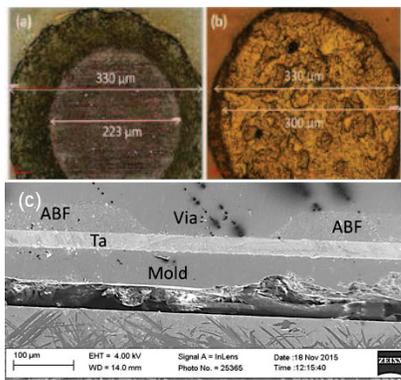

Figure 6.   Optical images (top view) of drilled via on (a) tantalum; (b) gold electrodes; and (c) cross-sectional SEM image of drilled via on tantalum electrode.
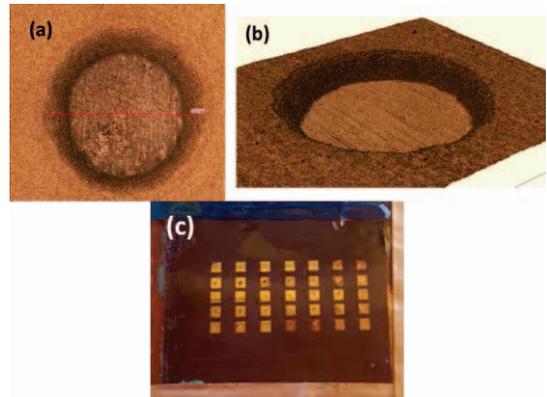

Figure 7.   (a, b) Optical images of partially filled vias; and (c) top image of integrated capacitor array on silicon.

TABLE II. ELECTROPLATING CONDITIONS

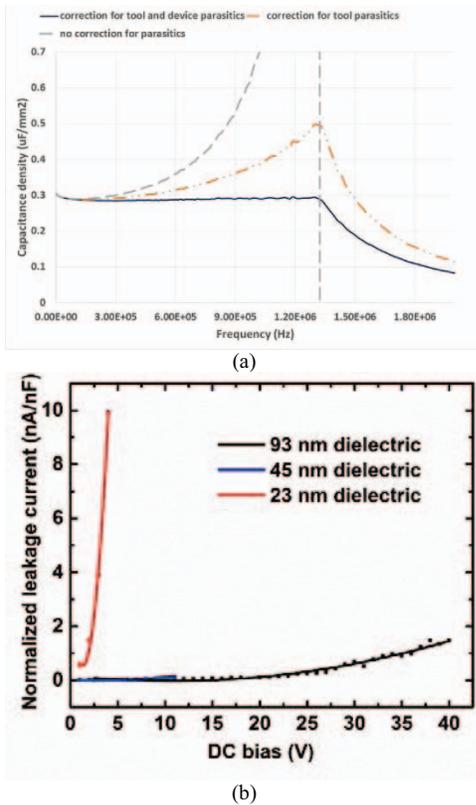| Parameters	Conditions
Bath temperature	30ºC
Current density	1A/dm²
Plating duration	30 min
Agitation	Air

(a)

(b)

Figure 8.   (a) Capacitance density vs. frequency for a thin-film tantalum capacitor; and (b) Leakage current for different dielectric.

Fig. 8(b) shows the normalized I-V plot for capacitors (with metal as top electrode) for dielectric thicknesses of 23 nm, 45 nm and 93 nm for capacitors with particle size of 300 nm. As expected, the thicker dielectric showed lower normalized leakage current (nA/nF) even at higher voltage as compared to thinner dielectric because of the relatively lower defect density. The thinnest dielectric showed the worst leakage characteristics due to leakage contributions from ion hopping, SCLC and Schottky mechanisms based on leakage models [18]. After leakage current measurements, the devices showed no change in capacitance for capacitors with either of the dielectric thicknesses, indicating the robustness of the dielectric.

The presence of thicker dielectric reduces the leakage current from close to 2.5 nA/nF to less than 0.05 nA/nF at 3V as the dielectric thickness was raised from 23 nm to 93 nm. The capacitance density was observed to be fairly consistent at ~0.3 μF/mm^2 for the entire range of DC bias from 1-5 V. It is important to note that the integration scheme did not degrade the electrical properties of the integrated capacitor in terms of the frequency and voltage stability of the capacitance density as well as the low leakage values. The large capacitance density at large operating frequencies would also require smaller capacitor foot-prints and lead to lower associated costs.

IV.   CONCLUSIONS

Thin high-density tantalum capacitors were fabricated and integrated on silicon. These ultra-thin capacitor arrays with a thickness of ~75μm demonstrated capacitance densities of 0.3μF/mm^2 at 5 MHz with low leakage current of 0.05 μA/μF at 3V. The capacitor integration process is designed to form thin tantalum capacitors on variety of substrates such as organic, glass, silicon or ceramics. These high-density, high-frequency tantalum capacitors enable highly-efficient, miniaturized and low-cost power modules.

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