Multi-scale thermal modeling of glass interposer for mobile electronics application

Sangbeom Cho
Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, Georgia, USA
Venky Sundaram and Rao Tummala
3-D Systems Packaging Research Center, Georgia Institute of Technology, Atlanta, Georgia, USA, and
Yogendra Joshi
Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, Georgia, USA

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Abstract

Purpose – The functionality of personal mobile electronics continues to increase, in turn driving the demand for higher logic-to-memory bandwidth. However, the number of inputs/outputs supported by the current packaging technology is limited by the smallest achievable electrical line spacing, and the associated noise performance. Also, a growing trend in mobile systems is for the memory chips to be stacked to address the growing demand for memory bandwidth, which in turn gives rise to heat removal challenges. The glass interposer substrate is a promising packaging technology to address these emerging demands, because of its many advantages over the traditional organic substrate technology. However, glass has a fundamental limitation, namely low thermal conductivity (~1 W/m K). The purpose of this paper is to quantify the thermal performance of glass interposer-based electronic packages by solving a multi-scale heat transfer problem for an interposer structure. Also, this paper studies the possible improvement in thermal performance by integrating a fluidic heat spreader or vapor chamber within the interposer.

Design/methodology/approach – This paper illustrates the multi-scale modeling approach applied for different components of the interposer, including Through Package Vias (TPVs) and copper traces. For geometrically intricate and repeating structures, such as interconnects and TPVs, the unit cell effective thermal conductivity approach was used. For non-repeating patterns, such as copper traces in redistribution layer, CAD drawing-based thermal resistance network analysis was used. At the end, the thermal performance of vapor chamber integrated within a glass interposer was estimated by using an enhanced effective thermal conductivity, calculated from the published thermal resistance data, in conjunction with the analytical expression for thermal resistance for a given geometry of the vapor chamber.

Findings – The limitations arising from the low thermal conductivity of glass can be addressed by using copper structures and vapor chamber technology.

Originality/value – A few reports can be found on thermal performance of glass interposers. However thermal characteristics of glass interposer with advanced cooling technology have not been reported.

Keywords Multi-scale, Thermal modelling, Interposer, Vapour chamber

Paper type Research paper

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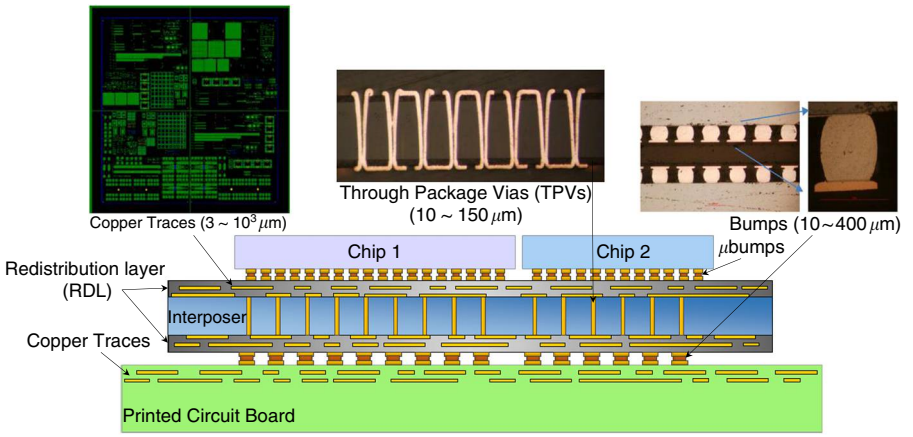
Nomenclature

a	width of vapor chamber	m, n	indices for summation
A	area	Q	heat flow rate
A_{copper}	total copper pixel area	R	thermal resistance
$A_{polymer}$	total polymer pixel area	R_{1D}	one-dimensional thermal resistance
$A_{row/column}$	pixel area for row/column thermal resistance	R_s	spreading resistance
A_s	heat source area	R_{total}	total thermal resistance
A_{total}	total pixel area	R_{vc}	vapor chamber total thermal resistance
A_0, A_m, A_n, A_{mn}	Fourier coefficients	A_s	heat source area
b	length of vapor chamber	t1	vapor chamber thickness
c	width of heat source	T_f	condenser cooling temperature
d	length of heat source	X_c,Y_c	heat source centroid
h	heat transfer coefficient	$\beta_{m,n}$, δ_n, λ_m	eigen values
k	thermal conductivity	θ_{jb}	junction to board thermal resistance
k_{copper}	copper thermal conductivity	$\overline{\theta}$	mean temperature excess ($T - T_f$)
k_{eff}	effective thermal conductivity	ϕ	spreading function
$k_{in\text{-}plane}$, $k_{x\text{-}y}$	in-plane (x-y direction) thermal conductivity	ς	dummy variable
$k_{out\text{-}of\text{-}plane}$, k_z	out-of-plane (z direction) thermal conductivity		
L_{total}	total pixel length		

1. Introduction

Mobile electronics are packing more features than ever before, and require higher bandwidth (10-30 GB/s) and larger memory capacity, with the same or lower power consumption. Additionally, the form factors of such devices continue to shrink, especially in thickness. In order to address these demands at a reasonable manufacturing cost, breakthroughs in packaging technologies are needed. 3D integrated circuit (IC) structures where multiple chips or dies are stacked have been considered to be an efficient solution to achieve these goals, but there still remains a number of technical challenges because of the large power density. Hence, interposers are considered as a good alternative for stacked integration technology. Interposer is a packaging platform with high density of electrical connections, and it is used to fan out the electrical connections to a wider pitch, and also to route the signals between different components placed on the same interposer. Because of the high wiring density, interposers can support large number of input/outputs (I/Os) required by the advanced IC technology nodes. Figure 1 shows the schematic of a so-called 2.5D glass interposer structure, where two dies are connected to each other through copper traces in the redistribution layer (RDL) on the interposer substrate, while both dies are connected to printed circuit board (PCB) through the copper plated through package vias (TPVs).

Silicon and glass are two major candidates for an interposer substrate. Silicon interposer has been developed to overcome the limitations of organic substrates due to many advantages, including high I/O density. However, it is limited to 300 mm wafer sizes, leading to high fabrication cost per interposer. Also, its high electrical losses due to its higher conductivity, limit its electrical performance. To address these issues glass



Note: Numbers in brackets are minimum and maximum sizes of the features in each component

Figure 1.
Schematics of 2.5D glass interposer structure

interposers are being developed (Sukumaran *et al.*, 2010). Glass has the advantage of panel-based processing, which results in lower cost per interposer. Combined with the advantages of ultra-high electrical resistivity, and low electrical losses, it becomes an excellent interposer candidate, especially for mobile applications (Sundaram *et al.*, 2014). However, glass has a thermal conductivity about 100 times lower than that of silicon. This limitation can potentially be overcome by incorporating copper structures and thin heat spreaders for the enhancement of thermal performance. A number of studies have investigated the thermal characteristics of interposers through simulation (Lau and Yue, 2009; Zhang and Zhang, 2015). Also, a few experimental thermal characterizations of interposer structures have been reported, and compared with simulations (Oprins *et al.*, 2011; Zhang *et al.*, 2014). Heinig *et al.* (2014) presented thermal analysis and optimization results for various 2.5D and 3D integrated processor configurations. These results indicated that maximum total power of the processor on 25 mm × 16 mm interposer can be increased up to 10 W when there is convective heat removal on bottom side with an effective heat transfer coefficient of 50 W/m^2K. Nonetheless, most of the previous works focus on silicon-based integration technologies and thermal studies on glass-based integration technologies are currently lacking (Cho *et al.*, 2013; Oprins and Beyne, 2014).

This paper is organized into three parts. The first part explains multi-scale modeling challenges in interposer modeling and explains the way TPVs, bumps and microbumps are modeled. The second part describes ways to simplify the copper traces in RDL and PCB for computational efficiency, and compares the effect of different copper structures on the thermal performance of glass and silicon interposers. In the third part, a vapor chamber integrated glass interposer is introduced and its thermal performance is characterized. The results from the vapor chamber simulations are compared with different copper structure simulations to quantify thermal performance enhancement.

2. Interposer thermal modeling and its length scale

As shown in Figure 1, interposers consist of microbumps, interposer substrate, TPVs, and bumps. Top and bottom surfaces of the interposer substrate are laminated with dielectric

layers, which work as buildup layers for wiring, referred to as RDLs. Complicated copper traces are buried in the layer and connected to enable communication between different chips mounted on the interposer. There are TPVs in the interposer substrate, which pass completely through the substrate for vertical electrical connection between chips and package substrate. The TPVs are either partially or fully filled with copper.

Length scales used for modeling 2.5D interposer range from several micrometers to tens of meter. Figure 1 and Table I compare the different length scales used in interposer modeling. When including all the fine details of interposers in the model results in need of extensive computational time and resources to solve the simulation. As such, a compact or reduced order modeling methodology is needed. Over-simplification of the geometric features, however, can produce large errors in the temperature profile. For this reason, compact modeling of interposer needs a balance between accuracy and computational efficiency. In this paper, different compact modeling schemes are used for different interposer components to develop computationally efficient and accurate thermal model.

3. Compact model for microbump/TPV/Bump modeling

Microbump/TPV/bump arrays are modeled by simplifying the geometry into an equivalent block with effective thermal conductivity. Figure 2 summarizes the compact modeling procedure used for TPV array. To begin with, a unit cell of TPV is chosen, and thermal boundary conditions to calculate effective thermal conductivity are applied to this cell. Out-of-plane (z direction) effective thermal conductivity is calculated by imposing uniform heat flux condition at top and negative heat flux at bottom

Table I.
Sizes used in interposer modeling

	Size (width(mm) × length(mm) × height (mm))
Chip	10 × 10 × 0.5
Interposer	25 × 25 × 0.2
Printed circuit board (PCB)	50 × 50 × 1.2

Note: Geometric dimensions of chip, interposer and printed circuit board (PCB)

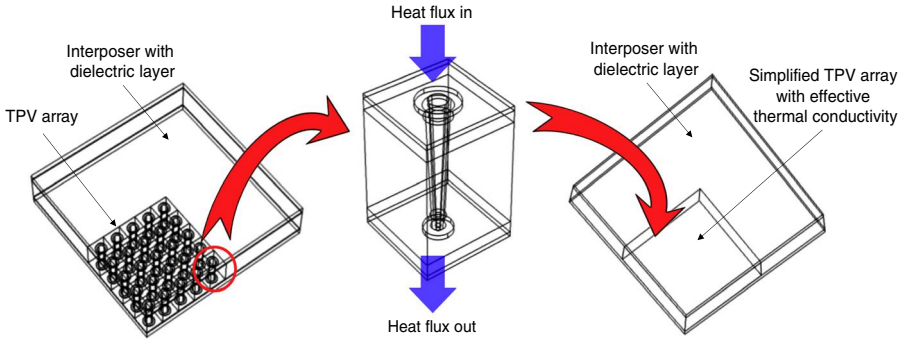


Figure 2.
Compact modeling scheme used for TPV modeling

Note: Upper part of TPV array is connected to microbumps, and lower part is connected to bumps

surface, while surrounding surfaces are set as adiabatic. The average temperatures of the top and bottom surfaces are obtained and consequently the equivalent thermal conductivity is calculated using:

$$k_{eff} = Q'' \frac{\Delta x}{\Delta T} \quad (1)$$

where Q″ is the heat flux, Δx the thickness of the sample, and ΔT the temperature difference across it. In-plane (x-y direction) effective thermal conductivity is calculated by applying the same boundary conditions to two side walls, while the other boundaries are kept as adiabatic. This approach averages local hot spot temperature, which may underestimate the peak temperature. However, using average die temperature is still a valid approach to evaluate and compare thermal characteristics of electronics packaging while a uniform heat generation is assumed. The approach was validated under uniform heat generation boundary condition by comparing the simplified model with detailed model, which showed only ~1 percent difference between maximum temperatures predicted by the two models (Cho *et al.*, 2013). More detailed validation of the approach under various geometric conditions is provided in the literature (Ma *et al.*, 2014). Material properties and the calculated effective thermal conductivities of interconnects and TPV s are shown in Table II.

4. Compact model for copper traces in RDLs

In a RDL, copper traces are patterned in a sophisticated way to enable I/O layout and the fan out from the chips to a looser pitch footprint. Such redistribution requires thin film polymers such as dielectric layers, and metallization to enlarge the pitch of the chip I/Os to match that of another array configuration with larger pitch. Figure 3 shows the top view of the example four metal layers with different patterns and cross-sectional view of TPV and copper traces patterned in a package substrate with single IC chip.

Figure 4 explains how in-plane effective thermal conductivity is calculated for metal layer with copper traces when the layers are assumed to be orthotropic. First, the CAD drawing of a metal layer is converted to a binary image, which contains the size and location information of the copper traces and the polymer. A black pixel in the figure represents copper, and the white pixel represents polymer. Then, the layout is divided into small tiles and each tile's total thermal resistance is obtained by using thermal resistance network analysis. Out-of-plane thermal conductivity of metal layer is calculated with the assumption that black and white pixels are thermally parallel. Pixel resolution of the

	k_{x-y} (W/m K)	k_z(W/m K)
Silicon	130	130
Glass	1	1
Polymer	0.8	0.8
Underfill material	0.7	0.7
Copper	400	400
PCB (FR4)	0.3	0.3
Microbumps	2.8	4.4
Bumps	1.8	4
TPV unit cell (glass)	1.2	33.7
TPV unit cell (silicon)	119.8	87.3

Table II. Material properties and calculated effective thermal conductivities of interconnects and TPVs

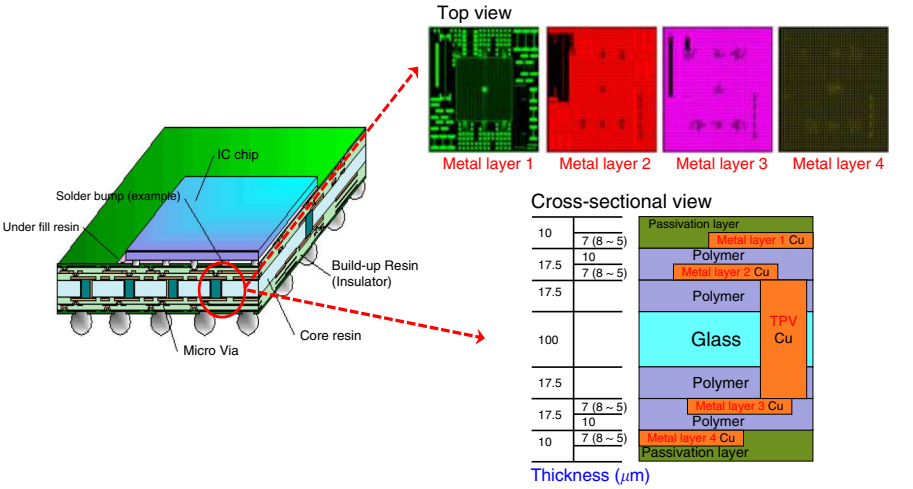


Figure 3.
Package substrate with single chip

Note: Top view of example metal layers' layout and cross-sectional view of TPV and metal layers (right)
Source: Left image from www.shinko.co.jp/english/product/buildup/dll.html

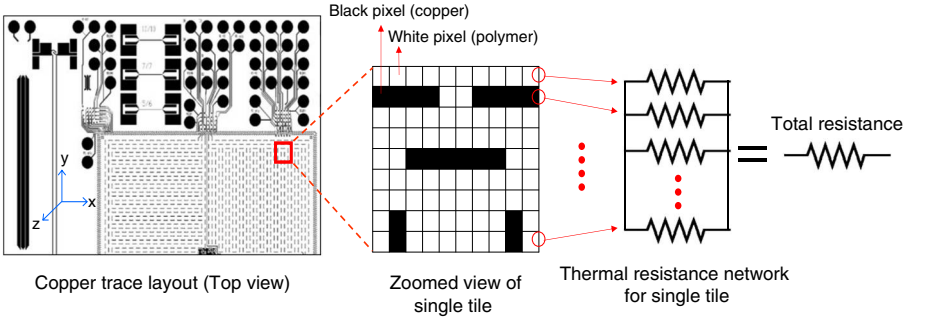


Figure 4.
Determination of total thermal resistance to obtain in-plane effective thermal conductivity for compact modeling of metal layer

image is considered to be acceptable when the difference between calculated effective thermal conductivity from current image and the highest resolution image that CAD program could export is less than 5 percent. Generally, 25 times reduction of pixels from maximum resolution results in ~4 percent difference between the results.

Equations (2) and (3) are used to calculate in-plane (row: x-direction, column: y-direction) and out-of-plane (z direction) effective thermal conductivity, respectively:

$$R_{row/column} = \frac{(Number\ of\ white\ pixels) \times (Pixel\ size)}{k_{polymer} A_{row/column}} + \frac{(Number\ of\ black\ pixels) \times (Pixel\ size)}{k_{copper} A_{row/column}} \quad R_{total} = \frac{1}{\sum (1/R_{row/column})}$$

$$k_{in-plane} = \frac{L_{total}}{A_{total}} \sum (1/R_{row/column}) \tag{2}$$

$$R_{total} = \frac{1}{1/R_{copper} + 1/R_{polymer}} \quad k_{out-of-plane} = \frac{A_{copper}}{A_{total}} \times k_{copper} + \frac{A_{polymer}}{A_{total}} \times k_{polymer} \quad (3)$$

The tile with complicated copper traces is then converted into a simple block with calculated thermal conductivities along x, y, and z direction. More details and the validation of this approach are presented in Blackmore (2009).

5. The effect of copper structures on glass and silicon interposers

Using the compact modeling schemes introduced above, the thermal models for 2.5D glass and silicon interposers are developed. Assuming that chips on the interposers are generating the same amount of heat (3 W) uniformly, and one ground plane is embedded in PCB, thermal performance of glass, and silicon interposers with different copper structures are compared. During the analysis, PCB bottom surface temperature is fixed at 300 K and other surfaces are assumed to be adiabatic. Four microbumps under the chip center area are assumed to be connected to a single TPV, and four TPVs are connected to single bump. Microbumps in the chip periphery area have finer pitch than those in center area to provide dense interconnection between two chips. Solder bumps are uniformly distributed at the bottom of interposer. Four metal layers are incorporated in the model, and identical metal layouts are used for both of the interposers. The schematic of the interposer structure and metal layer layouts are shown in Figure 5, and detailed geometric conditions for simulation are provided in Table III.

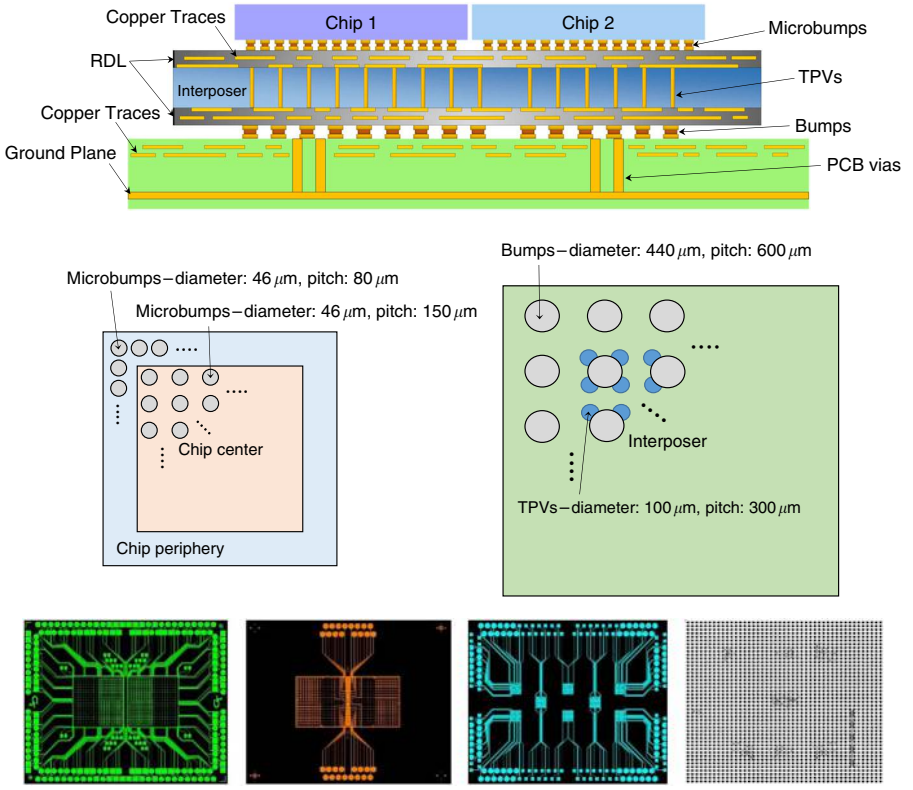


Figure 5.
The schematic of 2.5D interposer (top) microbump/bump/TPV layout (middle) and layouts of four metal layer (bottom) used for simulation

Figure 6 compares junction to board thermal resistance of glass and silicon interposers with different copper structure conditions at given boundary condition. The junction to board thermal resistance is determined by:

$$\Theta_{jb} = \frac{T_j - T_b}{Q} \tag{4}$$

where T_j is junction temperature, T_b is board bottom temperature, and Q is total heat generation rate from the chips. Table IV presents four different copper structure conditions applied when modeling TPV, RDL, and PCB. The thermal conductivities of RDL presented in cases 3 and 4 are the averaged values of thermal conductivities from four different metal layers in RDL. Incorporation of copper TPVs and copper ground layer improves thermal performance of glass significantly, making its out-of-plane effective thermal conductivity ~34 times higher than that of bare glass. Due to high thermal conductivity of silicon, the effect of TPVs and copper ground layer is not as significant in silicon as compared to the glass interposer case. Increasing in-plane effective thermal

Table III. Geometric dimensions of interposer components

	Length (mm)	Width (mm)	Thickness (μm)	Count
Chips	10	10	500	2
Interposer	25	25	200	1
PCB	50	50	1,000	1
Ground Plane	50	50	18	1
	Dimensions		Count	
Microbumps	ϕ: 46 μm, H: 33 μm		Center: 3,600 Periphery: 1,900	
TPVs	ϕ: 100 μm, H: 145 μm		900	
Bumps	ϕ: 440 μm, H: 270 μm		2,500	
PCB vias	ϕ: 400 μm, H: 700 μm		180	

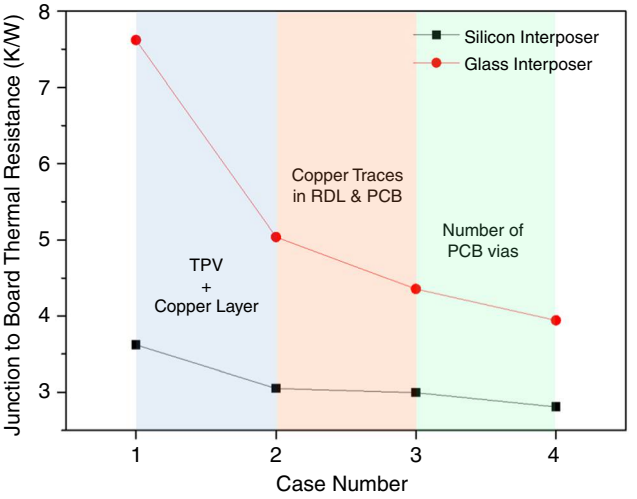


Figure 6. Junction to board thermal resistance of four different cases

Note: The factors that affect the thermal resistance are indicated on the plot

	TPV	RDL	PCB
Case 1	No TPVs	No copper k_{xy}, $k_z = 1$ W/m K	$k_{xy} = \sim 14$ W/m K No. of PCB vias: 180
Case 2	Table III	No copper k_{xy}, $k_z = 1$ W/m K	$k_{xy} = \sim 14$ W/m K No. of PCB vias: 180
Case 3	Table III	$k_x = 40$ W/m K $k_y = 50$ W/m K $k_z = 12$ W/m K	$k_{xy} = 30$ W/m K No. of PCB vias: 180
Case 4	Table III	$k_x = 40$ W/m K $k_y = 50$ W/m K $k_z = 12$ W/m K	$k_{xy} = 30$ W/m K No. of PCB vias: 360

Table IV.
TPV, RDL, and PCB conditions for four different cases

conductivities of RDL and PCB, or out-of-plane effective thermal conductivity of PCB by increasing number of PCB vias does not increase the performance of both interposers much. It is observed that the copper structure implementation has a significant effect on the thermal performance of glass interposer than that of silicon interposer.

6. Glass interposer with vapor chamber integrated PCB

In this part of the paper, the application of a vapor chamber to interposer structure is discussed and its effect on thermal performance is simulated. Figure 7 introduces the concept of vapor chamber integrated PCB for the interposer. A cavity formed in PCB is plated with copper and is covered with a copper lid, which is directly connected to PCBs. Heat generated from the chips flows through copper TPVs, and heats up the chamber's evaporator. The working fluid inside the chamber vaporizes at the evaporator, and limits temperature rise of the device. At the condenser, the vapor condenses back to liquid, which is attached to a large copper layer heat sink. A wick structure is used to provide the capillary action needed to drive the liquid against gravity. Thin layer of wick structure over evaporator area will potentially enhance liquid supply to the evaporator.

To develop a simplified vapor chamber integrated interposer model, the entire vapor chamber is modeled as a block with an effective thermal conductivity by using the thermal resistance of a vapor chamber with a similar geometry and boundary conditions obtained from literature (Ranjan *et al.*, 2012). An analytical expression for spreading resistance of a

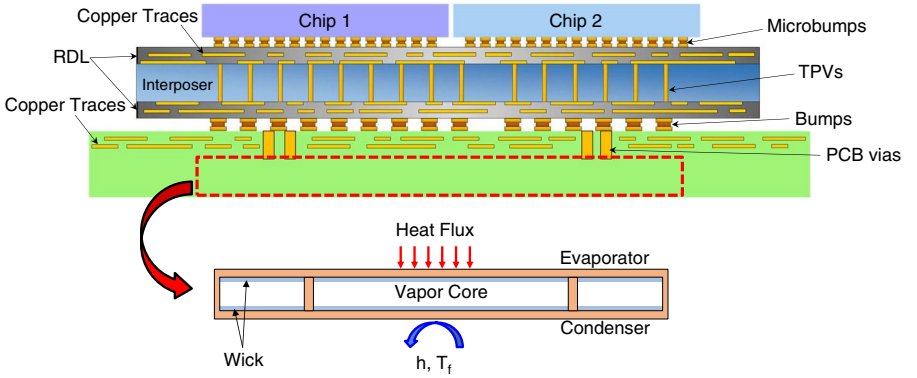


Figure 7.
Interposer with vapor chamber integrated PCB

three dimensional rectangular plate (30 mm × 30 mm × 1 mm) with single heat source (5 mm × 5 mm) shown in Figure 8 is utilized to extract effective thermal conductivity of a vapor chamber. To further simplify the model, the effective thermal conductivity of the vapor chamber structure was considered to be isotropic. The governing equation for the system shown in Figure 8 and its boundary conditions are:

$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}=0 \tag{5}$$

$$\left.\frac{\partial T}{\partial z}\right|_{z=0}=-\frac{Q/A_s}{k_{eff}} \quad \text{(within heat souce area: } A_s=cd\text{)} \tag{6}$$

$$\left.\frac{\partial T}{\partial z}\right|_{z=0}=0 \quad \text{(outside the heat source area)} \tag{7}$$

$$\left.\frac{\partial T}{\partial z}\right|_{z=t_1}=-\frac{h}{k_{eff}}\left[T(x,y,t_1)-T_f\right] \tag{8}$$

$$\left.\frac{\partial T}{\partial x}\right|_{x=0,a}=\left.\frac{\partial T}{\partial y}\right|_{y=0,b}=0 \tag{9}$$

The solution for the above differential equations can be obtained by using separation of variables. By integrating the solution, mean source temperature can be found as (Yovanovich *et al.*, 1999):

$$\begin{aligned}\overline{\theta}=\overline{\theta}_{1D}+\overline{\theta}_S=\overline{\theta}_{1D}&+2\sum_{m=1}^{\infty}A_m\frac{\cos(\lambda_m X_c)\sin\left(\frac{1}{2}\lambda_m c\right)}{\lambda_m c}\\&+2\sum_{m=1}^{\infty}A_n\frac{\cos(\delta_n Y_c)\sin\left(\frac{1}{2}\delta_n d\right)}{\delta_n d}\\&+4\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}A_{mn}\frac{\cos(\delta_n Y_c)\sin\left(\frac{1}{2}\delta_n d\right)\cos(\lambda_m X_c)\sin\left(\frac{1}{2}\lambda_m c\right)}{\lambda_m c\delta_n d}\end{aligned} \tag{10}$$

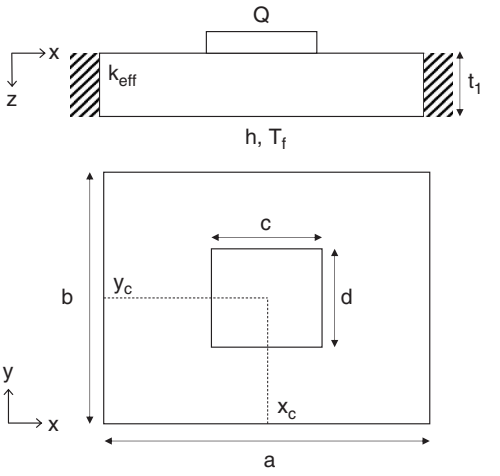


Figure 8.
Isotropic plate with rectangular heat source on top and boundary conditions for analytical expression of thermal resistance

where $\lambda = m\pi/a$, $\delta = n\pi/b$, $\beta = \sqrt{\lambda^2+\delta^2}$,

$$A_m = \frac{2Q\left[\sin\left(\frac{(2X_c+c)}{2}\lambda_m\right)-\sin\left(\frac{(2X_c-c)}{2}\lambda_m\right)\right]}{abck_{eff}\lambda_m^2\phi(\lambda_m)} \tag{11}$$

$$A_n = \frac{2Q\left[\sin\left(\frac{(2Y_c+d)}{2}\delta_n\right)-\sin\left(\frac{(2Y_c-d)}{2}\delta_n\right)\right]}{abdk_{eff}\delta_n^2\phi(\delta_n)} \tag{12}$$

$$A_{mn} = \frac{16Q\cos(\lambda_m X_c)\sin\left(\frac{1}{2}\lambda_m c\right)\cos(\delta_n Y_c)\sin\left(\frac{1}{2}\delta_n d\right)}{abcdk_{eff}\beta_{m,n}\lambda_m\delta_n\phi\left(\beta_{m,n}\right)} \tag{13}$$

$$\phi(\zeta) = \frac{\zeta\sinh(\zeta t_1)+h/k_{eff}\cosh(\zeta t_1)}{\zeta\cosh(\zeta t_1)+h/k_{eff}\sinh(\zeta t_1)} \tag{14}$$

where $\xi = \lambda$, δ, or β, and:

$$\overline{\theta}_{1D} = \frac{Q}{ab}\left(\frac{t_1}{k_{eff}}+\frac{1}{h}\right) \tag{15}$$

Finally, total thermal resistance of vapor chamber can be expressed as:

$$R_{VC} = \frac{\overline{\theta}}{Q} = \frac{\overline{\theta}_{1D}+\overline{\theta}_S}{Q} = R_{1D}+R_S \tag{16}$$

which can be expressed as a function of k_{eff}. By equating Equation (16) with the vapor chamber thermal resistance listed in the literature (Ranjan *et al.*, 2012), equivalent thermal conductivity k_{eff} was calculated. To find a solution, the Levenberg-Marquardt method, a damped least square minimization technique was used. After calculating the effective thermal conductivity, it was then used for developing finite element (FE) model of a simplified vapor chamber. After FE simulation, thermal resistance was calculated and the result was compared with the original thermal resistance value from the literature for validation, and two thermal resistance values showed ~2 percent difference. Upon validation, this effective thermal conductivity was then applied to the simplified block in PCB and used for performance estimation. Figure 9 summarizes the steps taken for simulation of interposer with vapor chamber embedded PCB.

Two thermal resistance values in the literature (Ranjan *et al.*, 2012), calculated from 1D resistance network analysis and numerical model, were used to calculate effective thermal conductivity of vapor chamber. The result is shown in Table V. Thermal resistance value obtained from the numerical model was used for effective thermal conductivity calculation, as the result from 1D resistance network analysis does not capture the vapor core resistance and underestimates the total resistance value.

Figure 10 shows the effect of vapor chamber and copper structures studied in this paper by including the thermal structures sequentially and comparing the thermal performance of glass interposer to that of silicon interposer for each of these cases. Different TPV, RDL, and PCB conditions used for cases 1, 2, and 3 can be found in Table IV. The previous result for case 4 in Figure 6 is now replaced by the result

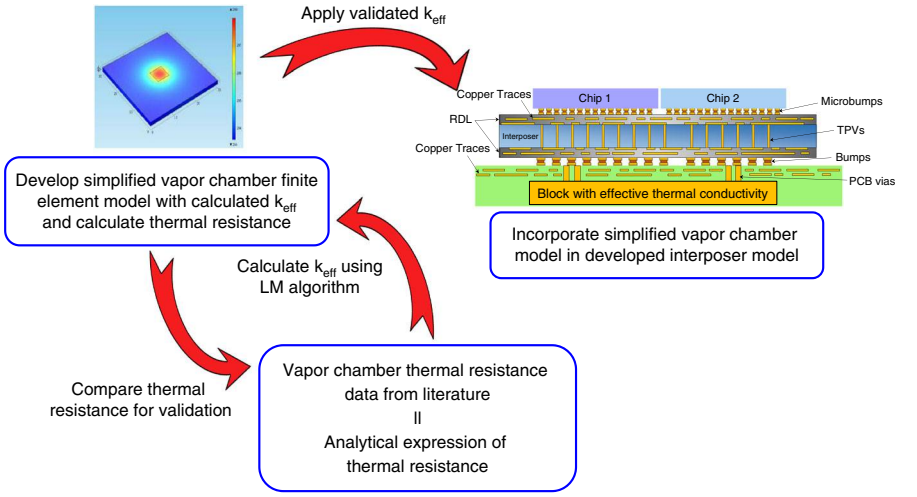


Figure 9.
Thermal performance simulation steps for interposer with vapor chamber integrated PCB

Table V.
Effective thermal conductivity of vapor chamber

	Thermal resistance (K/W)	Effective thermal conductivity (W/m K)
1D resistance analysis	0.27	1,526
Numerical model	0.51	491

Note: Calculated effective thermal conductivity based on thermal resistance

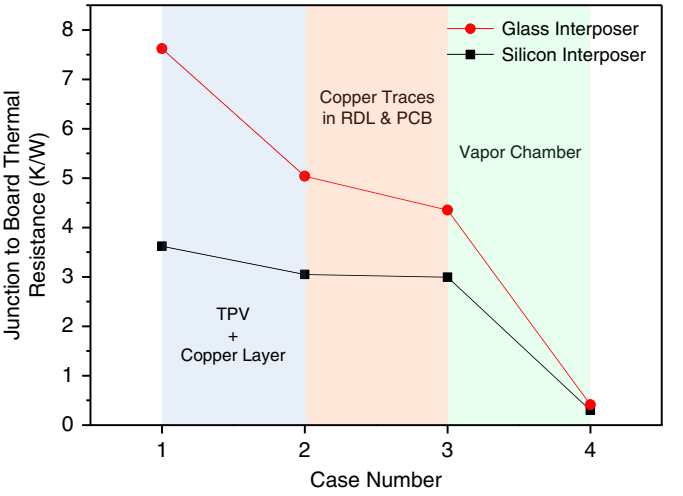


Figure 10.
Junction to board thermal resistance of four different cases

Note: The factors that affect the change of thermal resistance are indicated on the plot

from vapor chamber integrated interposer and shown in Figure 10. After the implementation of vapor chamber in both interposers, thermal resistance of glass interposer for case 4 is almost identical to silicon interposer, while the difference between the two interposers is significant for case 1. The vapor chamber in PCB, which provides better heat spreading effect than thin copper ground layer in PCB, offers significant thermal performance enhancement to glass interposer with thermal paths made by copper structures.

7. Conclusions

This study investigates the thermal performance enhancement of glass and silicon interposers through FE modeling. A 2.5D interposer model was developed to compare the effect of copper structures on silicon and glass interposers. Detailed interconnect and TPV geometry were incorporated to develop a more realistic model. Major results from the parametric design study are as follows:

(1) Different compact modeling schemes were used to address multi-scale modeling challenges in interposer modeling.

(2) The implementation of copper TPVs in interposer and copper ground layer in PCB, enhanced the thermal performance of interposers. TPVs work as thermal, as well as electrical paths.

(3) Comparing the effect of copper TPVs on glass and silicon interposers, TPVs in glass interposer work better as an effective thermal path than in silicon interposer. Glass isolates heat within the chip due to its low thermal conductivity. Silicon interposer substrate, however, spreads the heat which lowers the chip temperature efficiently.

(4) Thermal performance improvement affected by copper traces in RDL and PCB was studied. The thermal performance of glass and silicon interposers is affected more by the in-plane thermal conductivity of PCB, than that of RDL. A change in in-plane thermal conductivity of RDL on silicon interposer has negligible effect on the thermal performance of the interposer. Overall, enhancements in out-of-plane thermal conductivity more significantly affect thermal performance, than that in the in-plane thermal conductivity.

(5) Further improvement in thermal performance can be achieved through the implementation of vapor chamber in PCB. Glass and silicon interposers show almost identical performance with vapor chamber, overcoming the low thermal conductivity of glass.

(6) During the simulation, both silicon and glass interposers were assumed to have the same geometric features and conditions. However, as shown in Figure 11, whenever silicon is used as interposer, an additional packaging layer needs to be added to address thermal stress caused by coefficient of thermal expansion mismatch, which adds an additional thermal resistance to the system. When glass interposer is used, there is no need for this additional layer, which can make thermal performance of glass interposer comparable or better than silicon interposer with vapor chamber. This also gives more compactness in packaging to glass interposer, making it more suitable for small form factor electronic systems, than silicon interposer.

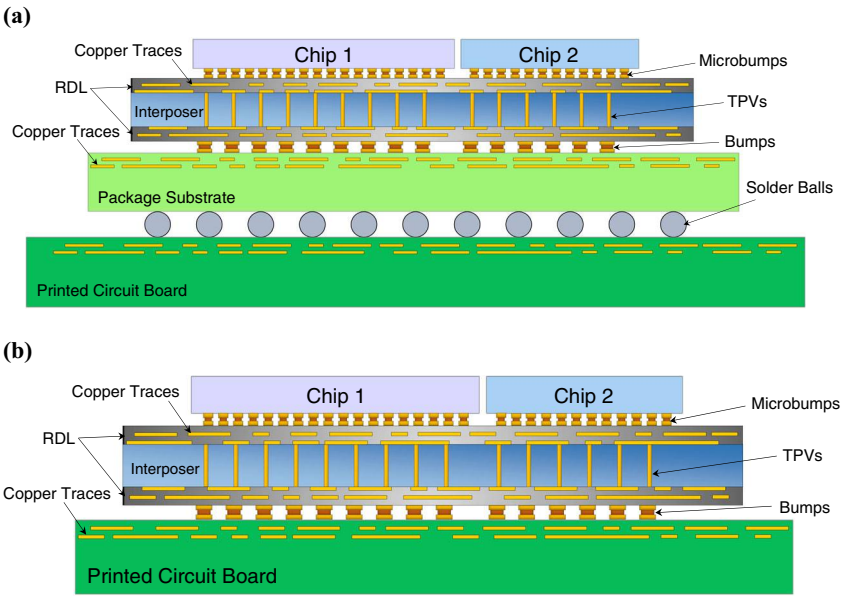


Figure 11.
(a) Silicon interposer geometry with additional packaging layer, and (b) Glass interposer geometry

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Corresponding author
Yogendra Joshi can be contacted at: yogendra.joshi@me.gatech.edu