Thermocompression Bonding Process Design and Optimization for Warpage Mitigation of Ultra-thin Low-CTE Package Assemblies

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Abstract—**Increasing needs for functionality, performance and system miniaturization in fine-pitch consumer applications have been driving a new class of ultra-thin interposers and packages with larger body sizes, aggravating warpage. These trends gave rise to serious concerns for assembly yield and reliability, especially at board level. The recent adoption of substrate technologies with silicon-matching coefficient of thermal expansion (CTE) reinforces these concerns by introducing a large CTE mismatch between package and organic board. Warpage control and mitigation in assembly has, therefore, become critical in enabling reliable SMT interconnection of ultra-thin, large, low-CTE BGA packages to the board. Copper pillar thermocompression bonding (TCB) has emerged as a key assembly technology to improve die assembly yield at pitches below 80μm and large die sizes. In TCB, heat is applied from the die side only while the substrate is maintained at a low stage temperature, as opposed to isothermal heating in mass reflow. The temperature gradient in the package can, therefore, be finely tuned providing control over the warpage behavior.**

This paper investigates TCB-induced warpage and its dependence on the bonding thermal profiles in a single-chip, 200μm-thick, low-CTE organic package at 50μm pitch and 17mm x 17mm body size. Warpage trends as a function of the stage temperature were first predicted with a simple coupled thermal-structural finite-element model, then experimentally validated by Shadow-Moiré measurements of assemblies built with varying stage temperatures from 70ºC to 150ºC. Interactions with the thermocompression tool, in particular the effect of vacuum-coupling of the substrate to the stage, were considered and investigated. Guidelines for design of TCB profiles for warpage minimization were finally derived with considerations of assembly throughput to improve board-level SMT yield and system-level reliability.

Keywords- low-CTE packages; warpage; thermocompression bonding; finite-element simulation; reliability; Cu pillar

I. INTRODUCTION

Recent advances in packaging have been driven by emerging consumer and high-performance applications. These applications constantly need higher bandwidth and transmission speed at lower power and low cost, as well as for increased functionality and miniaturization. These requirements translate into key technology trends, including I/O pitch scaling, increased interconnect densities and die sizes, raising reliability concerns at chip-level due to the large CTE mismatch between silicon and conventional laminates [1, 2]. This mismatch causes severe warpage during die assembly, leading to increased strains in the solder interconnections, and subsequently degrading the fatigue life [3]. A new class of ultra-thin, low-CTE interposers and packages was introduced to address these warpage and reliability challenges. These low-CTE silicon, glass or organic substrates possess relatively high elastic modulus and stiffness at elevated temperatures, displaying ssignificant performance and reliability improvements at chip level [4, 5]. Reduction in substrate thickness, to below 300μm, however, aggravates its propensity to warp, degrading yield and reliability.

Low-CTE silicon and glass interposers have recently gained momentum in trending 2.5D and 3D system architectures, requiring substrate technologies that can support high-density wiring at sub-5μm interconnect pitches [6, 7]. Such interposers typically exceed 30mm x 40mm in size, further aggravating warpage concerns. At such large body sizes, low-CTE substrates face critical reliability challenges if assembled directly to the board. To overcome these challenges, now at board level, a three-level hierarchy was established in which the semiconductor devices are mounted on the high-density interposer, then connected to an organic package, SMT-attached to the board. If this three-level hierarchy helps in redistributing pitch and mitigating CTE mismatch to improve thermo-mechanical reliability, warpage mitigation in assembly of these large interposer packages remains a grand challenge, yet to be fully addressed by the semiconductor industry.

System-level warpage, yield and subsequent reliability were found mostly governed in 2.5D interposer packages by the assembly sequence and unit process conditions [8]. In particular, better control over substrate warpage and its minimization has been demonstrated with thermo-compression bonding as compared to mass reflow, through careful design of thermal and force profiles [9-11]. In TCB, heat is typically applied from the die side only with a constant stage temperature maintained throughout the process. Such heating profile serves two purposes: 1) achieving high throughput on account of rapid heating and cooling of the small chip element at rates up to 400K/s, which are fundamentally impossible. to reach with bulky stages; and 2) enabling the use of pre-applied underfill

materials (PAMs), typically epoxy-based non-conductive pastes directly patterned on substrates, which require low stage temperatures, below their thermal stability on stage temperature of 70ºC to 90ºC [10]. Die bonding at higher stage temperatures was shown to provide a reduction in warpage of silicon interposers by over 40% [8]. In this CTE-matched assembly, elevating the stage temperature reduces the thermal gradient between chip and interposer at the solidification point of the solders from which mechanical coupling, and hence warpage, originates. Alternative interconnection technologies, such as low-temperature solders or compliant interconnections, have also been explored to minimize warpage in interposer-to-package assembly [12][13]. However, this interposer-package architecture is sub-optimal due to the need for an additional package layer limiting the electrical performance and increasing the thickness and the cost of the system. Solutions for direct SMT assembly of large, ultra-thin 2.5D packages are therefore highly sought after, and can only be enabled through fundamental understanding of the individual and combined effect of each assembly step.

This paper addresses warpage mitigation challenges by design and optimization of thermocompression bonding processes through a) accurate thermomechanical finite element modeling of TCB processes, focusing on the effect of the thermal profile, b) using these models to estimate substrate warpage at package level, c) validating the models with comprehensive experimental results, and d) mitigating assembly warpage based on these models to achieve superior system-level reliability. A basic 2D single-chip package was used for this focused study to extract key parameters and trends for warpage control in TCB.

II. TEST VEHICLE DESIGN AND FABRICATION

Daisy chain test vehicles at 50μm pitch were used in this study. The silicon test die, 7.3mm x 7.3mm in size, and 200μm in thickness comprised 528 Cu pillar interconnections in a single peripheral row. The bumps were 30μm in diameter, and composed of Cu pillars, 30μm in height, a Ni barrier layer of approximately 2μm and a SnAg solder cap, 12μm in height. The test die with peripheral arrangement is shown in the picture of Figure 1, while Figure 2 gives the detail of the Cu pillar interconnection stack-up. The low-CTE substrates, 17mm x 17mm in size, supplied by Walts Co. LTD, consisted of a copper-clad, 200μm-thick MCL-E-679FG type S organic core by Hitachi Chemical with a CTE of 3.3ppm/K. The first copper wiring layer was patterned by subtractive processing. Dielectric ABF-GX-3 build-up layers from Ajinomoto were then laminated to support a second layer of copper wiring, formed by double-side semi-additive processes. Dry-film solder mask was then applied with an 80μm-wide slit opening in the bonding area, exposing fan-in fan-out bump-on-trace finger structures, as shown in Figure 3. Electroless nickel immersion gold (ENIG) surface finish was finally plated on the exposed traces. The substrate stack-up design is recapped in Table I.
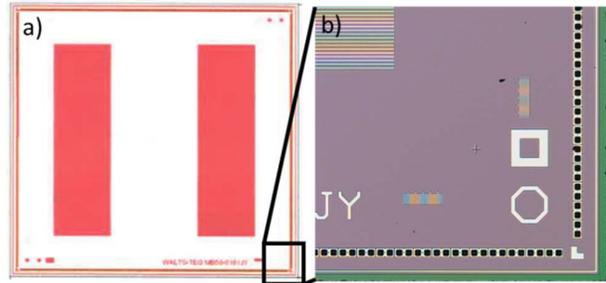

Figure 1. Daisy chain test die at 50μm pitch: a) design and b) optical image of a bumped corner (Walts Co. LTD).
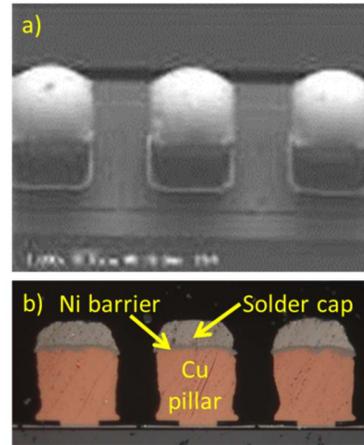

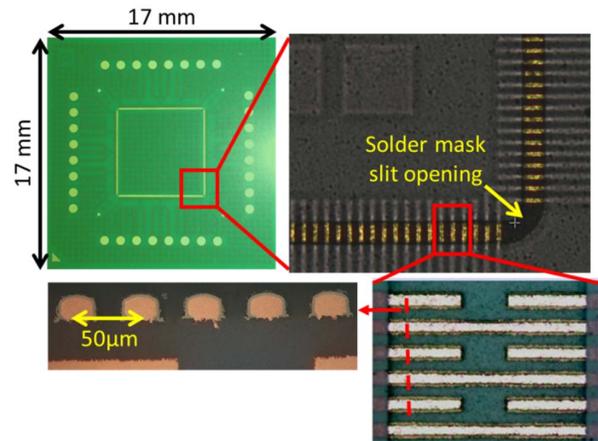Figure 2. Cu pillar interconnections at 50μm pitch: a) top view, and b) cross-section.

Figure 3. Low-CTE organic substrate with bump-on-trace wiring (Walts Co. LTD).

TABLE I. SUMMARY OF SUBSTRATE STACK-UP DESIGN
(COURTESY OF WALTS).

	Thickness (mm)	Material
Solder Resist (on Pattern)	0.015	PSR4000-AUS703
Pattern	0.015	Copper
Insulating Layer (Built up Material)	0.030	ABF-GX-3
Pattern	0.018	Copper
Base Core	0.200	Base Core Material E6979FGS
Pattern	0.018	Copper
Insulating Layer (Built up Material)	0.030	ABF-GX-3
Pattern	0.015	Copper
Solder Resist	0.015	PSR4000-AUS703

III. FINITE-ELEMENT MODELING

Finite-element models were created to understand the effect of bonding conditions, in particular of the stage temperature, on warpage of the substrate. Modeling was done in ANSYS™ 15.

Ideally, 2.5D or 3D models are desirable in order to evaluate the results accurately. However, 2D models with plane strain approximation are appropriate for comparison between different assembly processes based on the geometry of Figure 4. The mesh was refined at the solder and thin layers. As we move away from the critical regions, the mesh was coarser and the number of elements as compared to the thickness was built to sufficiently capture warpage. An example of the model mesh is depicted in Figure 5. The low-CTE substrate, polymer dielectric layers, copper redistribution layers, copper pillar interconnections, and silicon die were included in the model. The die-substrate assembly represents a cut along the diagonal with symmetry boundary conditions at the center. The node at the left bottom was fixed in the y-direction to prevent rigid body motion. A simple elastic model was used for the solder because the effect of a more accurate model is negligible on warpage. Material properties used in the model are given in Table II.
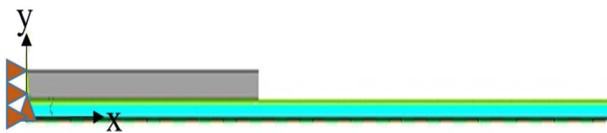

Figure 4. Example geometry in modeling. Two-dimensional geometry represents a cut along the diagonal of the package with symmetry at the left.
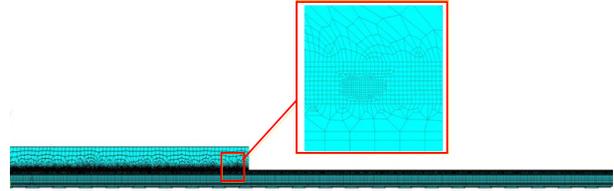

Figure 5. Example mesh used in modeling for thermal and mechanical analysis.

TABLE II.   MATERIAL PROPERTIES USED IN MODELING

Material	E [GPa]	CTE [ppm/ºC]	ν	Stress-Free Temp. [C]
Silicon chip [14]	$E_{x,z}$ = 169 E_y = 130	2.6	0.28	220
SAC 305 Solder [15]	47.6	24	0.36	220
Low-CTE core	36	3.3	0.12	160
Copper [16]	59.2-80	17	0.33	200
Polymer	5	39	0.34	150

Coupled thermal-structural finite-element models were constructed to predict the temperature gradient in the package during TCB (Figure 6). The solution from the thermal gradient was then used as reference for each material element, and then fed as input to the mechanical model.
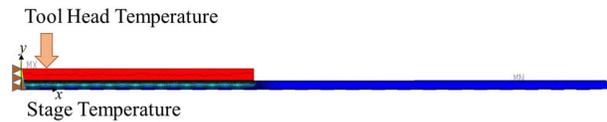

Figure 6. Example of thermal gradient in the package during TCB.

The solution steps for the four-metal layer package includes the application of a thermal gradient across the package, applying a cooling model from solder melt temperature to room temperature and feeding the solution to a mechanical model that calculates the displacement in y-direction. This simulation mimics the warpage during assembly process. The substrate bottom was simulated to be heated at temperatures varying from 70°C to 150°C and the die top correspondingly from 360°C to 305°C, with sufficient thermal budget to melt the solder in every condition. The model was solved and the predicted warpage was plotted as a function of the stage temperature in Figure 7.
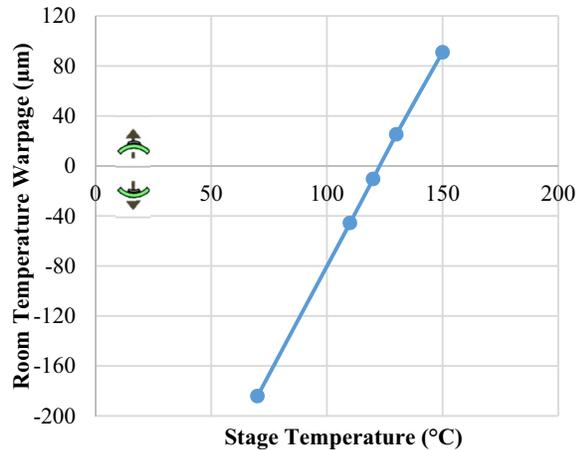
Figure 7. Predicted warpage as a function of stage temperature for a low-CTE organic package.

The warpage plot predicts that there is a change in direction of warpage with increasing stage temperatures. This change occurs at temperatures beyond 120°C. At higher stage temperatures, the magnitude of warpage continues to increase, but in the opposite direction. These predictions correlate well with observations in silicon-to-silicon bonding, showing lesser warpage at higher stage temperatures [8]. An example of warpage prediction at 70°C stage temperature is shown in Figure 8.

Figure 8. Predicted warpage of low-CTE package assembled using 70°C stage temperature conditions.

IV. ASSEMBLY

The test vehicles described in Section II were assembled by dip-flux thermocompression bonding using a semi-automatic Finetech Fineplacer Matrix flip-chip bonder with a placement accuracy of ±3μm. The conventional underfilling step was skipped in this study as variability in fillet size have been shown to have a strong effect on substrate warpage and thus needs to be decoupled and studied separately [17]. The TCB force and thermal profiles were designed by varying the tool head peak temperature and dwell time at a given stage temperature, heating and cooling ramp rates, and applied force. The bonding conditions were optimized based on systematic electrical yield analysis by DC measurements of the as-bonded daisy-chain resistances, and die-shear testing followed by qualitative observation of the fracture profiles and solder spread on the traces.

A fine control of the solder spread on the trace was found critical in achieving good yield. Due to the slit passivation opening and the lack of confinement that a PAM would provide, the solder is free to flow on the

exposed trace during the process. Excellent wettability of the ENIG surface finish creates a driving force for solder lateral spread, leading to its depletion from the joints if not restricted. This mechanism is illustrated in Figure 9. (a) (b), showing the cross-sections of a yielded and non-yielded samples, respectively. As interdiffusion rates are much higher in liquid phase, lateral spread of the solder is mostly governed by the duration spent above its melting point that needs to be precisely controlled. Such fine control is challenging with the lab-scale bonder used in this study, due to the slow achievable ramp rates with a maximum of 6K/s compared to 400K/s in production. An increase by only 1°C of the tool peak temperature was found to degrade the yield from all 45 connected daisy chains, to only three corner chain readings. Proper melting and wetting of the solder was obtained with tool head peak temperatures of 360°C, 340°C, 325°C and, 305°C, corresponding to stage temperatures of 70°C, 90°C, 120°C and, 150°C, respectively, with no dwell time at peak temperature. The force profile was optimized along the thermal one, with an initial 1N force applied until reaching a temperature in the solder of approximately 150°C, then released to 0.5N during reflow.

To study interactions with the bonder, in particular coupling effects with the stage induced by vacuum holding of the substrate, assembly was carried out with and without vacuum in the same conditions. To virtually strengthen the vacuum hold, the substrates were taped to the stage with Kapton® tape. At least two samples were bonded in the same conditions to give representative trends for TCB-induced warpage.
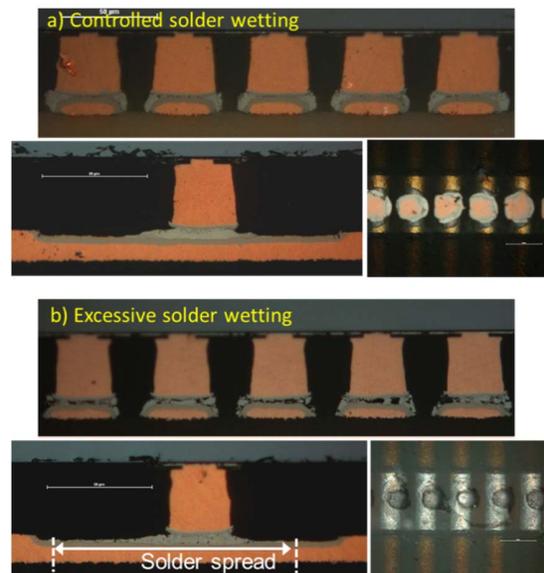

Figure 9. Cross-sections and P-lap cross-section of: a) yielded assembly with controlled solder, and b) non-yielded assembly with excessive solder lateral spread.

V. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. Warpage Measurements

Substrate warpage was measured by Shadow-Moiré using Akrometrix's Thermoiré PS200S. Details on Shadow-Moiré can be found in various publications [18-20]. Warpage is defined as the difference between the highest and lowest points on the package after tilt has been accounted for. Warpage was measured over a temperature range of 25°C to 260°C from the substrate side. For each bonding condition, two or three samples were measured. The error margin of the tool and grating used is ± 1.5 µm. For warpage convention, the "frown" shape (die is on top) is positive and the "smile" shape is negative, as indicated by the icons in Figure 7.

Figure 10 shows a typical warpage curve evaluated by Shadow Moiré for the 70°C stage temperature bonding process. On heating, the warpage increases with increasing temperature since the substrate expands at a higher rate than the silicon. Above 200°C, the solder is in molten state and provides no mechanical coupling between the die, causing the warpage to decrease.
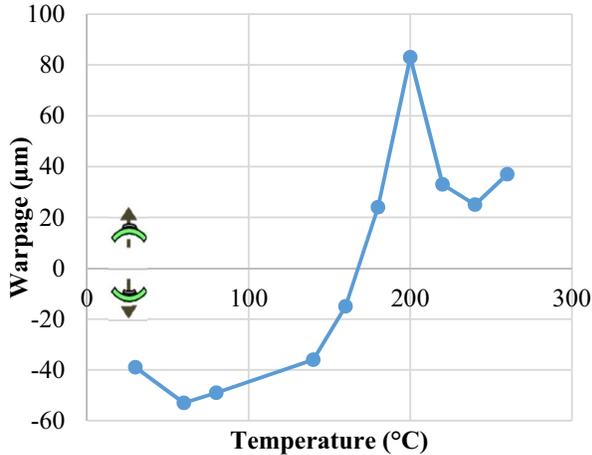

Figure 10. Package warpage as a function of temperature for TCB profile with 70°C stage temperature.

B. Effect of TCB Stage Temperature Without Substrate-Stage Coupling

Assembly was performed without coupling the substrate to the stage and the resulting room temperature warpage minus the unassembled substrate warpage is shown in Figure 11 as a function of stage temperature. It is seen that room temperature warpage for the 70°C stage temperature assembly condition is a smile-shaped warpage with higher magnitude than that at 90°C and 120°C. This is because the thermal gradient in the package when the solder is frozen is larger, which means the die has a larger temperature drop to room temperature and the substrate has a smaller temperature drop to room temperature. As the stage temperature is increased, the die head temperature is decreased, varying the thermal excursion in the package. In the 150°C stage temperature case, the substrate contracted more than the die, resulting in positive or frown-shaped warpage. Between the substrate shrinking more (150°C stage temperature case) and the die shrinking more (70°C, 90°C, and 120°C stage temperature cases), there exists a balance point where the different thermal excursions offset the CTE mismatch between the package and die and result in minimum net warpage. Therefore, based on the trend observed in Figure 11, the minimum warpage can be controlled by finely tuning the TCB profile.

Overall, the trend observed for TCB assembly without coupling between the substrate and stage was the same as was predicted in modeling (Figure 7). In both theory and experiments, the stage temperature to minimize warpage was about 120°C.
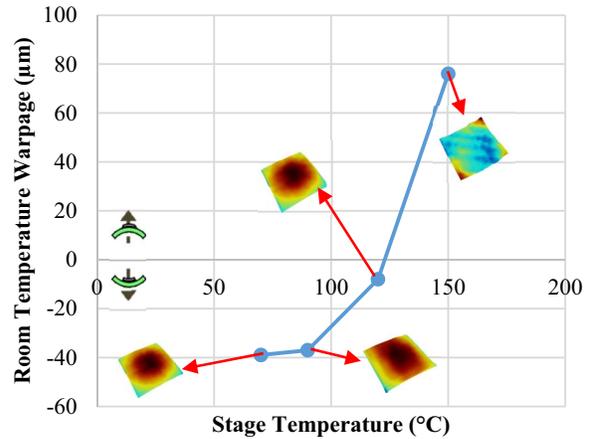

Figure 11. Room temperature package warpage as a function of stage temperature without coupling the substrate to the stage.

C. Effect of TCB Stage Temperature With Substrate-Stage Coupling

Assembly was performed with coupling between the substrate and stage and the resulting room temperature warpage minus the unassembled substrate warpage is shown in Figure 12 as a function of stage temperature. The coupled case showed smile-shaped warpage with similar magnitude for temperature gradients from 70°C and 150°C stage temperature bonding profiles. This result is different from the uncoupled case (Figure 11), which shows increasing room temperature warpage with increasing stage temperature. The only difference between the two cases was the coupling applied between the stage and substrate.

Why the coupled and uncoupled cases produce different trends is not yet fully understood, though there are several possible factors which play a role. Mechanically coupling the substrate and stage means that the substrate cannot warp during the bonding process. While pressure is applied to the die during the TCB process, the region outside the die is free to warp in the uncoupled case. Hence the substrate warpage is different between the coupled and uncoupled cases. Also, the coupling to the stage may be preventing further expansion of the substrate during assembly, which would

produce strain in the opposite direction as the thermal contraction. There may be thermal differences between the coupled and uncoupled cases as well. In the coupled case, the substrate is better adhered to the stage, lowering the contact resistance, and changing the thermal gradient when the solder freezes.

The relatively small change in room temperature warpage based in the coupled case implies that the temperature profile applied during TCB has little effect on the resulting warpage. Previous literature [13] has reported yield changes based on the temperature profile, which indicates that the temperature conditions should have an effect, however, the coupling effects were not studied.
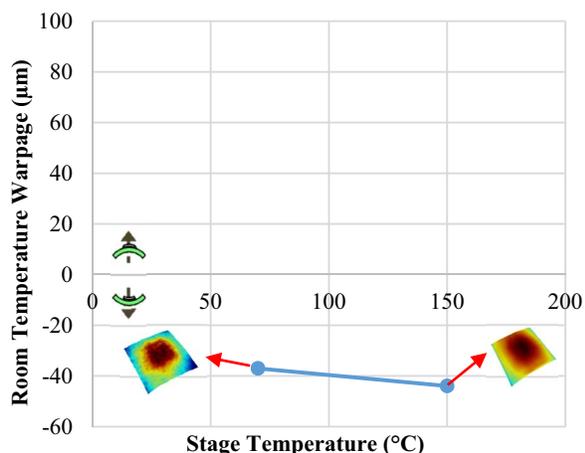

Figure 12. Room temperature package as a function of stage temperature warpage with coupling the substrate to the stage.

D. Discussion

In TCB, higher stage temperature is desired because it increases throughput by reducing the amount of time necessary for heating and cooling during the assembly process. For example, comparing 70°C and 150 °C stage temperatures with 200°C/s heating rate on a 7s process, the 70°C stage temperature requires ~6% more time from heating alone.

While the work in this paper used flux and no underfill for simplicity and to enable larger temperature ranges in TCB, it is common to use pre-applied underfill materials. When using PAMs, the effect these materials have on the thermal gradient and substrate-die coupling as well as the bonding profile requirements such as temperature and pressure must be taken into account. Non-conductive pastes (NCP) have limited thermal stability and must be kept at lower temperatures, which limits the stage temperature to 90°C and below. Non-conductive films (NCF) can be laminated on wafers, therefore allowing a higher stage temperature and consequently higher throughput.

VI. CONCLUSIONS

This paper demonstrates a process design approach for mitigating warpage induced by thermocompression bonding on ultra-thin, low-CTE substrates at I/O pitches below 50μm. By selecting optimum thermal profiles for mitigating chip-level assembly warpage, board-level assembly is enabled at larger package sizes, and system-level reliability is enhanced.

Finite-element models were developed to predict warpage based on the temperature profile applied during thermocompression bonding. Dies were then bonded with flux on low-CTE substrates with stage temperatures in the 70°C to 150°C range. When the substrate was not coupled to the stage, the room temperature warpage matched the theoretical predictions, showing increasing warpage with increasing stage temperature, with a smile-shape at low stage temperature and frown-shape at high temperature. In other words, the net or absolute warpage first decreases, then increases. To improve yield of board-level assembly and system-level reliability, minimum absolute warpage is desired, and net warpage for was predicted and experimentally found to be about 120°C.

Assembly was also performed with the substrate coupled to the stage over the same temperature range, and it was found that the bonding temperature profile had little effect on the room temperature warpage. Thus, in uncoupled assembly, it is possible to minimize warpage for improved yield and system-level reliability by finely tuning the temperature profile. However, this may not be possible when the substrate is tightly coupled to the stage. The reason why the coupled assembly behaves differently is presently being investigated.

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