Demonstration of 20 µm I/O pitch RDL using a novel, ultra-thin dry film photosensitive dielectric for panel-based glass interposers

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Abstract

This paper demonstrates, for the first time, a high density, low cost redistribution layer (RDL) stack-up using a novel, ultra-thin dry film photosensitive dielectric material for panel scale 2.5D glass interposers and fan-out packages. The salient features of this semi-additive process based RDL demonstrator include : (1) A two metal layer RDL structure with integration of 5 µm microvias at 20 µm pitch and escape routing of 2 µm Cu traces at 4 µm pitch. (2) 5 µm microvias fabricated using low cost i-line 365 nm UV photolithography process in ultra-thin 5 µm dry film photosensitive dielectric. The new photosensitive dielectrics, IF4605 (5 µm thick) and IF4610 (10 µm thick) in discussion, are primarily epoxy polymer based dry films. Epoxy resin is the standard polymer dielectric used in conventional package substrates today. Also, IF films have low dielectric constant and low curing temperatures as is the case with conventional epoxy dielectrics. This paper will demonstrate a multi-layer RDL stack with IF dry film for 20 µm I/O pitch interposers or fan-out packages. The panel based sputtering approach will be used to deposit Ti and Cu as the barrier and seed layers respectively. This also ensures high yield and reliability of the fine pitch Cu traces. The reliability of fine pitch Cu photovias are currently being evaluated for thermal cycling tests (TCT). Initial results are presented in the paper.

Keywords: Ultra-thin Dry Film Photosensitive Dielectric, Ultra-Small 5µm Photovias at 20 µm pitch, Thermal Cycling Reliability, 2.5D Panel-based Interposers, Fan-Out Packages

I. INTRODUCTION

System on Package (SoP) technology is gaining wide-spread attention in the recent times due to limitations in the scaling of Moore's law for integrated circuits. Also, the cost challenges involved in System on Chip (SoC) concept with respect to yield of fabrication, time and resources involved in the design of SoCs have led to SoP being more accepted by the industry. 2.5D Silicon Interposers by Xilinx [1], Embedded Multi-Die Interconnect Bridge (EMIB) technology by Intel [2] for very high performance systems like cloud computing and fan-out package technologies like Integrated Fan-Out (InFO) by TSMC[3] for ultra-miniaturized, multi-functional systems like mobile devices developed recently can all be considered as the upcoming era of SoP concept. However, all these SoP technologies are currently being processed on a 300 mm wafer scale. The size of these packages need to increase for higher number of heterogeneous integration of ICs in the coming future. This needs to be achieved at a lower cost, especially for consumer sensitive applications like fan-out packages for mobile devices. Hence, panel-based processing seems to have a promising future despite the number of challenges it faces today and a trend has been ongoing for 610 x 457 mm^2 panel level fan-out packages. [4] This paper tries to address some of the challenges associated with high-density RDL technologies for panel-based processing.

Semi-additive process (SAP) technology is the current front-up approach for RDL stack-up in high density packages. Shimizu et.al [5] demonstrated organic multi-chip integrated thin-film high-density organic package (i–THOP) substrate with BEOL wafer processes at ultra-fine feature sizes. In addition, Mitsuya Ishida [6] demonstrated advanced APX organic interposers with SAP based RDL using high number of metal layers (5-2-5 stack-up) and featuring 6 µm wide Cu traces and 20 µm diameter microvia processes. However, in all these cases, the panel scale-up of glass interposers or fan-out packages is limited by fine pitch, low cost RDL technologies. These limitations include: (1) Lack of ultra-thin, dry film polymer dielectrics with very low surface roughness for high yields of fine pitch (< 5 µm) Cu traces (2) Low cost, mass via generation methods for ultra-small microvias (< 10 µm) on a panel scale. This paper addresses both these challenges for panel scale and low cost SAP based RDL technology.

As a core material, glass serves as a promising solution for such panel scale systems due to its excellent electrical properties, exceptionally smooth, flat surface and high dimensional stability for precision lithography. Recent advances in panel-based RDL include embedded trace technology using excimer laser for obtaining high yields of fine pitch Cu traces. However, this embedded trace technology suffers from critical challenges like uniform Cu plating, throughput of excimer laser and removal of excess plated Cu from the dielectric surface. Excimer laser ablation technology is another advancement in the microvia drilling process. Suzuki et.al [7] demonstrated fabrication of 10 µm microvias using excimer laser ablation in 10 µm thick dielectric films. However, the high cost associated with the throughput of excimer laser is still a concern.

This paper highlights a novel, ultra-smooth and ultra-thin photosensitive dielectric IF dry film to address the above

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discussed challenges. Photovia technology using conventional i-Line 365 nm UV radiation has been known to be a promising, low cost solution for mass via generation in dry film polymer dielectrics. However, the main challenge has been the availability of a high resolution, ultra-thin dry film photodielectric material with ideal properties suited for panel level applications, which is the highlight of this paper.

This paper will demonstrate a two metal RDL stack-up with 10 µm IF4610 dry film for 20 µm I/O pitch interposers. The smallest Cu trace is 2 µm wide and via diameter is 5 µm. The panel based sputtering approach will be used to deposit Ti and Cu as the barrier and seed layers respectively. This also ensures the high yield and reliability of fine pitch Cu traces. The reliability of fine pitch Cu photovias are currently being evaluated for thermal cycling tests (TCT).

II. MATERIAL PROPERTIES OF IF FILM

The material properties of post-cured IF dry film are summarized in Table 1. The new photosensitive dielectrics, IF4605 (5 µm thick) and IF4610 (10 µm thick) in discussion, are epoxy based chemically amplified negative tone material which was originally designed and developed photopolymer for permanent structure fabrication used in Micro Electro Mechanical Systems (MEMS) field. Epoxy resin is the standard polymer dielectric used in conventional package substrates today. Similar to the conventional epoxy dielectrics, IF films have low dielectric constant and low curing temperatures. The IF film's curing condition is 200^0C for 1 hour and the cured polymer has a dielectric constant of 3.5 at 1 MHz . Also, as shown in Fig 1, IF4610 has very low average surface roughness (R_a) of < 5 nm and low R_z (average of five highest peaks and lowest valleys over the entire sampling length) of < 20 nm, comparable to the smooth polyimide films. This makes the film ideal for fabrication of high yield fine pitch Cu traces (< 5 µm) with sputtered Ti-Cu seed layer using panel-based sputtering tools. The high thermal stability of the film enables it to be an ideal candidate for the top layer passivation film of the package substrate as well. The highlight of the IF film is its excellent resolution. The films are shown to resolve vias as small as 2-3 µm. The dielectric film IF with its low modulus and high elongation break (20%) is very useful for good stress absorbance and long term reliability.

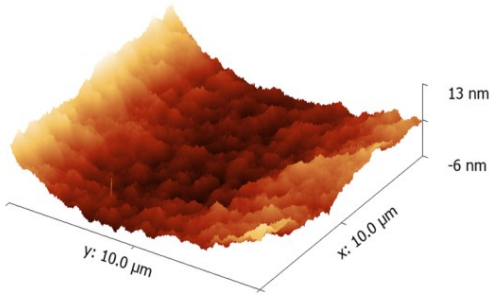

Fig 1. Surface Roughness of IF4610 Film

Properties	Measurement method	IF4610
T_g (°C)	DMA	250
CTE (ppm/°C)	TMA	45
Thermal weight loss temperature (°C)	TG/DTA	315 (3%)
		325 (5%)
Elongation to break (%)	Tensilon	20
Tensile strength (MPa)		82
Young's modulus (GPa)		1.64
Dielectric constant	CV, 1MHz	3.5
Loss Tangent	0.1 MHz	0.022

Table 1: Material Properties of cured IF4610 dry film

III. PATTERNING IN IF4610 FILM

The patterning in IF film is performed using the conventional semi-additive process. The process flow is described briefly in Fig 2. The first step in this process was lamination of the IF4610 film followed by photolithography to pattern the vias in the photodielectric.

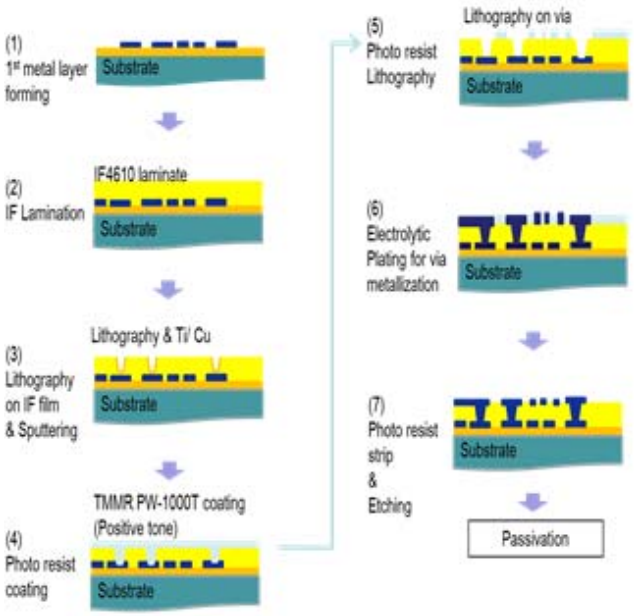

Fig 2. Semi-additive Process Flow for Multi-Layer RDL in IF4610 Film

The photolithography process for patterning 5 µm vias in IF4610 material is summarized in Fig 3. These steps include:

(A) Vacuum Hot Press lamination of IF4610 film on a substrate
(B) UV exposure(365 nm i-line) and post exposure bake process (90°C for 5 min)
(C) Development by the developer solvent PGMEA (Propylene glycol monomethyl ether acetate) and then thermal curing (200 °C for 1hr)

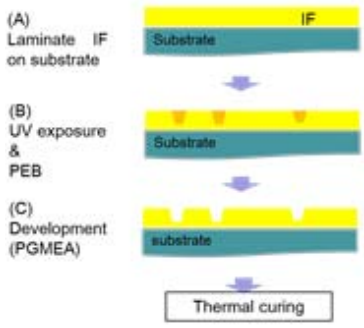

Fig 3. Photolithography Process in IF4610 film

Once the photovias were fabricated, a thin Ti-Cu barrier and seed layer was sputtered using PVD tool. Ti thickness was around 30 nm and Cu seed thickness was around 200 nm. Then, the liquid photoresist, TMMR P-W1000T®, was used for patterning of fine Cu traces. This was followed by Cu electroplating to fill the vias and Cu trace thickness of 3-4 µm was achieved. The immediate next step was photoresist stripping and followed by seed layer etching process. Differential Cu etchant was used to etch the Cu seed and dilute HF was used to etch the Ti seed.
Fig 4 below shows the typical resist profile of TMMR P-W1000T® after patterning a 2 µm Cu trace at 4 µm pitch.

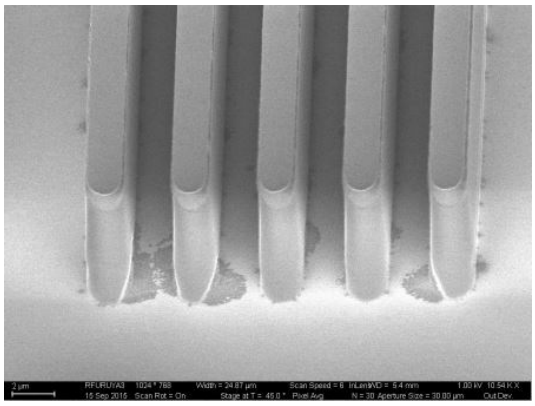
Fig 4. TMMR P-W1000T® resist profile for 2/2 µm L/S

To study the metallization performance of TMMR P-W1000T®, Ti-Cu seed was sputtered on a Si substrate and the substrate was patterned with 6 µm thick TMMR P-W1000T®. 3-4 µm of Cu was plated followed by seed layer etching step. Fig 5 shows the SEM images of the patterned metal traces. The ultra-low R_a and R_z of IF film, as noted in the material properties section, helps to replicate the same ultra-fine Cu trace patterns on a smooth IF4610 film as shown in Fig 6.

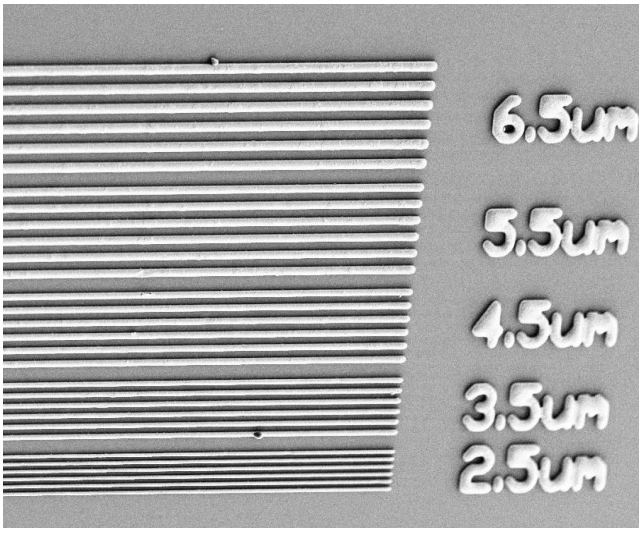

Fig 5. Metallized Cu patterns using TMMR P-W1000T®

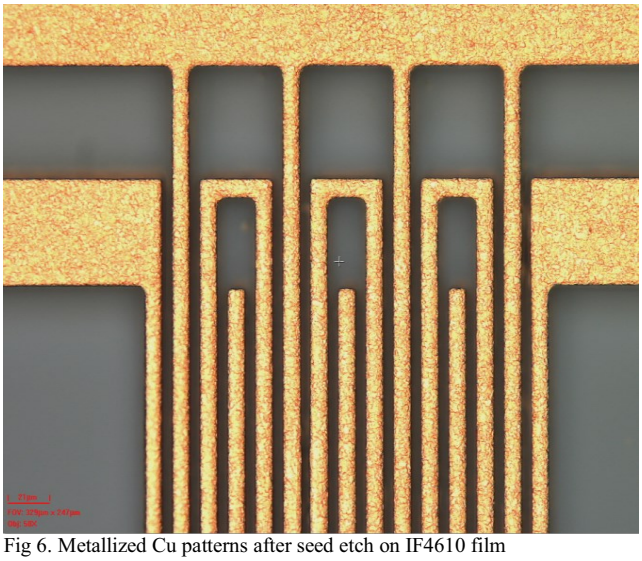
Fig 6. Metallized Cu patterns after seed etch on IF4610 film

Another highlight of the IF film, as previously noted, is its very high resolution for formation of ultra-fine photovias. Cu seed was sputtered on a smooth glass substrate and IF4605 film was laminated on the Cu seed layer. An advanced projection stepper, UX-44101 from Ushio Inc., was used for fine line and via photolithography. This tool is uses a high power i-line (λ = 365nm) light source and has 2 µm resolution in a 100 mm diameter or 70mm x 70mm large-panel exposure area. The alignment accuracy over this large-panel exposure shot is ±1 µm. The tool has ± 10 µm depth of focus (DOF) to accommodate for substrate warpage and thickness non-uniformity. Using UX-44101, 3-5 µm photovias were formed in the IF4605 film as shown below in Fig 7.

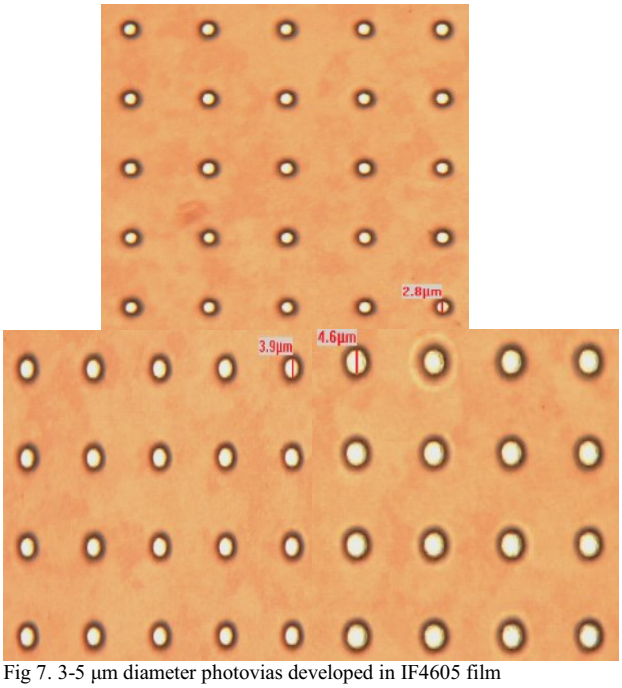

Fig 7. 3-5 µm diameter photovias developed in IF4605 film

IV. MULTILAYER RDL INTEGRATION AT 20 µm I/O PITCH USING IF4610 DRY FILM

The two metal layer RDL stack-up was achieved by conventional SAP technology. The process flow is similar to that described in Fig 2. The minimum width of the Cu trace routed was 2 µm at 4 µm pitch and the minimum diameter of the photovia fabricated was 5 µm at 20 µm pitch. Liquid TMMR P-W1000T® was used as the photoresist for patterning of fine Cu traces and sputtered Ti-Cu seed was used as the conductive seed layer.

Fig 8 shows the top view SEM images of the routed Cu traces with 5 µm vias integration at 20 µm I/O pitch while Fig 9 shows the integration at 40 µm I/O pitch.

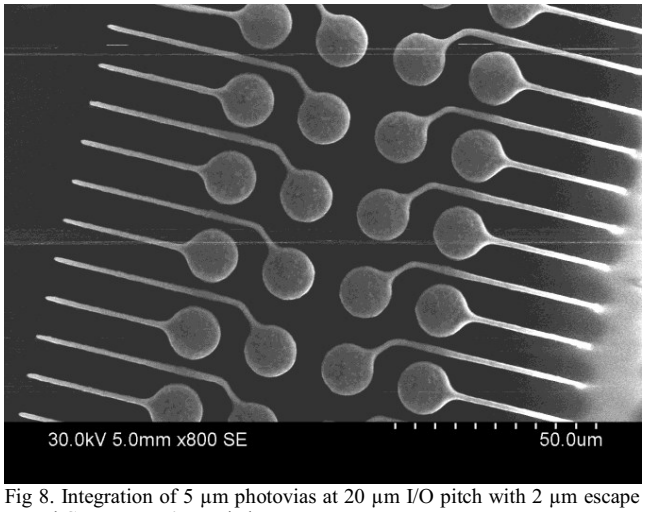

Fig 8. Integration of 5 µm photovias at 20 µm I/O pitch with 2 µm escape routed Cu traces at 4 µm pitch

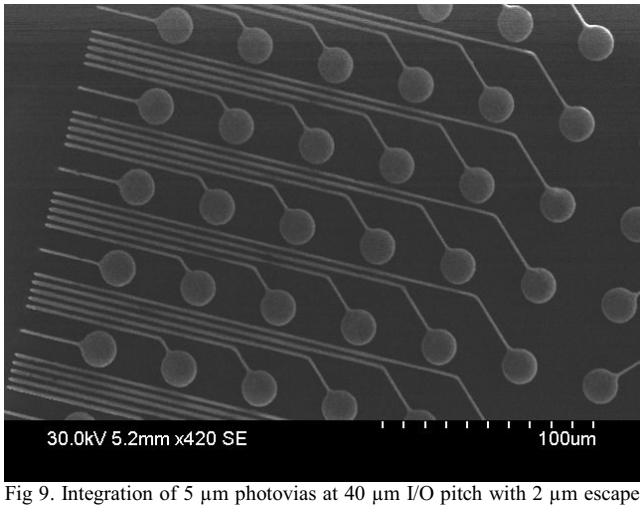

Fig 9. Integration of 5 µm photovias at 40 µm I/O pitch with 2 µm escape routed Cu traces at 4 µm pitch

Fig 10 shows the cross section image of the RDL integration at 40µm I/O pitch. This clearly shows the high density of metal Cu traces that can be escape routed due to the small via diameters achieved using IF4610 photodielectric film.

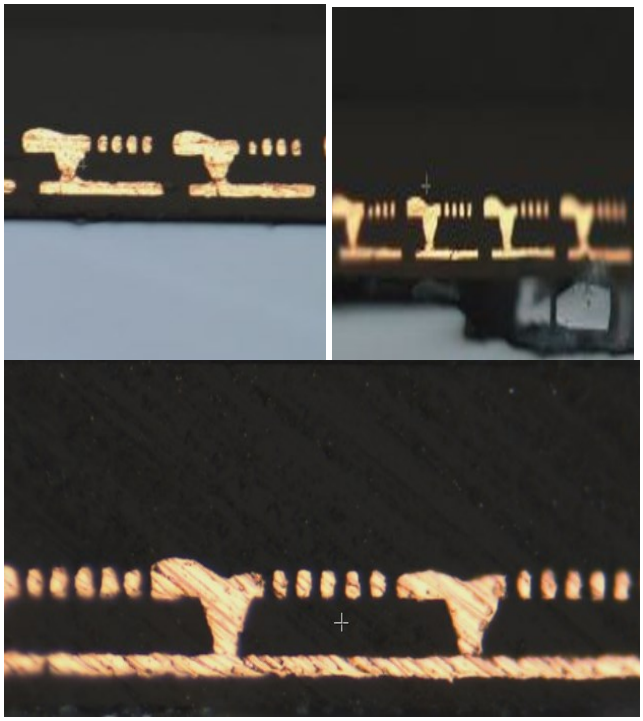
Fig 10. Cross section images of 5 µm photovias at 40 µm I/O pitch with 2 µm escape routed Cu traces at 4 µm pitch

Thus, a two metal layer, high density RDL integration was successfully achieved using SAP panel-based process using IF4610 dry film photodielectric polymer at 20 µm and 40 µm RDL via to via pitch.

V. RELIABILITY STUDIES OF RDL ON IF4610 FILM

Reliability Studies of 5 µm photovias at 20 µm pitch

The electrical resistance of ultra-small 5 µm photovias fabricated at 20 µm pitch was measured. Fig 11 shows the design structure of the daisy chain for 5 µm vias at 20 µm via-to-via pitch. Fig 12 shows the SEM image of the top view of the daisy chain structure and Fig 13 shows the plated structure of fully filled Cu vias. PVD Ti-Cu sputtered seed with Ti thickness of 30 nm and Cu thickness of 200 nm was used as the conductive seed layer to metallize the via structures in IF4610 film using conventional SAP technology.

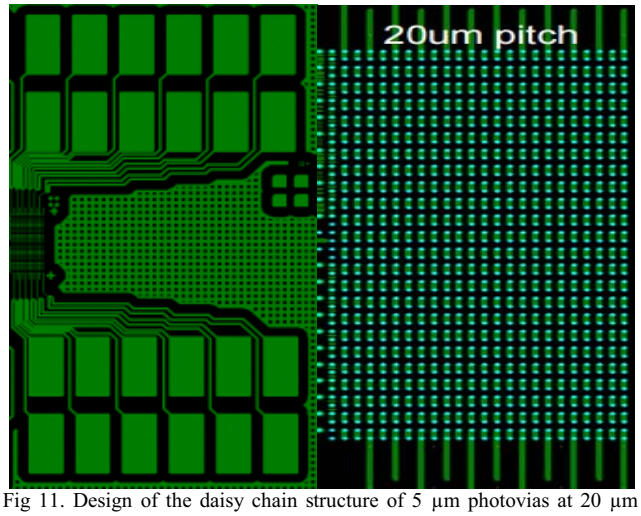

Fig 11. Design of the daisy chain structure of 5 µm photovias at 20 µm pitch

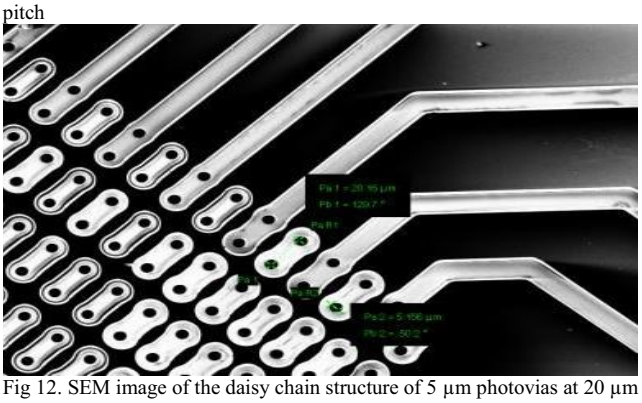

Fig 12. SEM image of the daisy chain structure of 5 µm photovias at 20 µm pitch

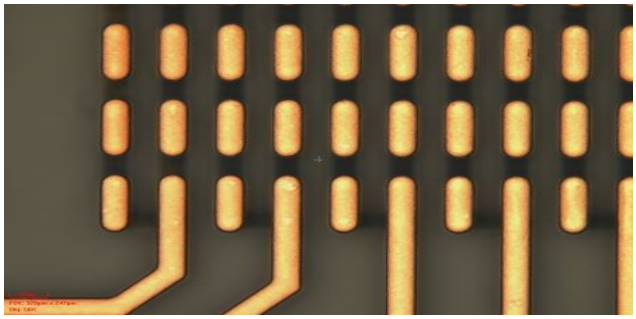

Fig 13. Daisy Chain structure of fully filled 5 µm photovias at 20 µm pitch

Once the daisy chain structure of the vias was fabricated, the samples were exposed to a thermal cycle reliability test. Pre conditioning for the daisy chain via structure according to Moisture Sensitivity Level 3 (MSL-3) test was first carried out. This was followed by JEDEC standard conditions for Thermal Cycling Test. MSL-3 test includes prebake at 125^0C for 24 hours to remove all the moisture in the samples and then moisture soaking was done in a humidity chamber at 60^0C, 60%RH for 48 hours followed by three cycles of solder reflow process with a peak temperature of 260^0C. The samples were kept in the thermal chamber for a holding time of 10 mins each at $+125^0$C and -55^0C. The failure criteria for drop in resistance after 1000 such thermal cycles is $\Delta R > 10\%$. The tests are currently ongoing and the initial resistance measurements are reported in Figure 14 below. Both 5 µm and 10 µm photovias shown in the plot below are at 20 µm pitch. As seen in Fig 11, the long trace lengths and the corresponding thin traces associated with the daisy chain vias are responsible for a relatively higher resistance measured at 20 µm pitch. Hence, we are interested in the relative increase (> 10%) of resistance after thermal cycling in this study and not the absolute values of resistances. The absolute values of resistances are affected by the thin and long trace pads associated with the daisy chain vias.

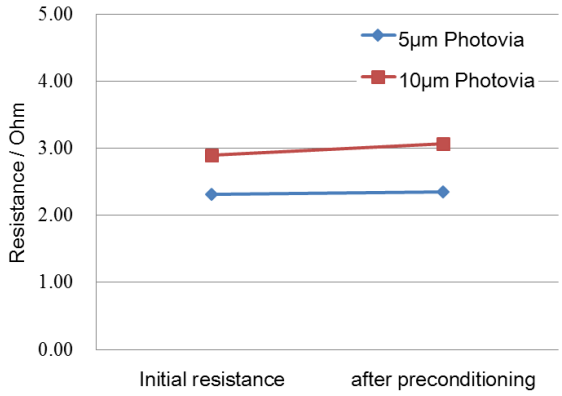

Fig 14. Initial Resistance Measurement for the via daisy chain structures at 20 µm pitch

VI. SUMMARY AND CONCLUSION

The limitations in the scaling of Moore's law have pushed System on Package (SoP) for future scaling of systems. There is a promising future for panel-based technologies to process substrates at low cost and high performance for ultra-miniaturized devices. Today's sequential build-up technology based on SAP is currently the front-up approach for the panel-based process. Other alternatives like laser embedded trench approach overcomes some of the challenges of SAP. However, some of the other challenges in terms of costs related to the throughput of excimer laser ablation processes,

surface plating and etching of excess Cu from the dielectric still remain with the embedded trench approach. This paper addresses some of the challenges with panel-based processing by introducing low cost, mass production capable ultra-small 5 µm photovias using a novel, ultra-thin (5 µm and 10 µm thick) epoxy based photosensitive dielectric IF film. The vias are fabricated using the conventional i-line 365 nm UV photolithography process. With PVD Ti-Cu seed and the ultra-smooth surface of the IF film, 2 µm Cu traces were demonstrated at 4 µm pitch. This work pioneers the demonstration of a high density RDL configuration based on semi-additive processing (SAP) featuring 5 µm photovias at 20 µm I/O pitch integrated with 2 µm escape routed Cu traces. This new generation RDL technology can be used for panel based 2.5D glass interposers and high-density fan-out packages at panel scales.

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