Next Generation Panel-Scale RDL with Ultra Small Photo Vias and Ultra-fine Embedded Trenches for Low Cost 2.5D Interposers and High Density Fan-Out WLPs

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***Abstract*—This paper presents a novel, high density, and large panel compatible thin film redistribution layer (RDL) process, with 2 µm diameter microvias and 2 µm fine line and space Cu traces on a thin glass panel using a photo-lithographic embedded trench approach. Newly developed thin dry film photosensitive polymer dielectrics were used for the fabrication of photo-vias and photo-trenches by conventional i-line 365 nm UV lithography in this work. Smallest feature dimensions of 1.5 µm trace widths and spaces were achieved by using liquid photosensitive polymer dielectrics. Such a high density, panel scale RDL is applicable to both high performance 2.5D interposers and high-density fan-out packages. The photo embedded trench process retains the cost advantages of the conventional semi-additive process (SAP) while overcoming its scaling challenges. The photo embedded trenches integrated with photovias using a thin, dry film photodielectric have higher resolution, precise via registration, and lower cost compared to the existing embedded trench methods. A dual-layer photo trench process was proposed and developed to address the challenges of copper plating uniformity in vias, pads and trenches. A test coupon consisting of six area array test structures with via diameters ranging from 2 to 5 µm at 20 µm pitch and lines and spaces of 2.5, 3, and 5 µm were designed and demonstrated on a 100 µm thin panel glass substrate. The 5 µm wide features was designed to capture vias within the trenches for a padless multi-layer RDL structure, with via diameters close to the line width enabled by the improved dimensional stability of glass compared to organic laminates. A new type of configuration, via-in-trench, with higher routing capacity than dog-bone or via-in-pad structures, was proposed and demonstrated on thin glass panels based on the photo embedded trench technology. Routing structures of line-space-via-trench (L, S, Via, T) of 3, 3, 3, 5 and 2.5, 2.5, 2, 2.5 µm on thin glass substrates were demonstrated without the use of via capture pads.**

Keywords-RDL; embedded trench; glass interposesr; fanout bump pitch; microvia

I. INTRODUCTION

2.5D silicon interposers with TSVs, starting with Xilinx's VIRTEX-7, have demonstrated the benefits of bandwidth, power and system integration enabled by high density RDL wiring. The critical dimension (CD) for VIRTEX-7 was 0.4µm using 65nm back-end-of-line (BEOL) wafer processes. Recently, dual damascene and thin film RDL processes have been applied to fan-out wafer-level-packages (FOWLP) to eliminate the electrical loss coming from silicon and TSVs, using so-called SLIT (Silicon-Less Interconnect Technology), SLIM (Silicon-Less Integrated Module) and SWIFT (Silicon Wafer Integrated Fan-out Technology) technologies by Xilinx, SPIL and Amkor.[1, 2] Although several wafer-based approaches have been demonstrated for 2-5 µm Cu trace RDL, panel processes used in flip-chip organic substrates and embedded chip substrates, have not been able to scale to ultra-fine lines and spaces below 6 µm. The photo trench process on glass panels presented in this paper provides a superior alternative, a low cost and high density wiring solution for 2.5D interposers and Fan-out RDLs.

Embedded trench processes overcome the limitations of semi-additive process (SAP) by eliminating the critical seed layer etching step and improving the reliability issues of fine traces.[3, 4] Laser embedded trench approaches using UV laser or excimer laser have been demonstrated for 12 µm and 8 µm lines and spaces in ABF dielectric films.[3, 4] The photo trench approach has demonstrated line width and space down to 1.5 µm by using liquid photosensitive dielectric.[5] Novel 5 µm (IF4605) and 10 µm (IF4610) ultra-thin, photosensitive dry films with high resolution were developed recently as RDL dielectric materials and used in this research, along with a projection Aligner, UX-44101, to create fine trenches and small vias by lithographic processes.

Multilayer RDL wiring capacity is not only dependent on line and space but also on the via diameter, via landing accuracy and capture pad size. Hence, microvias play as important a role as lines and spaces in RDL wiring density. Current laser ablation technology in production has reached 20 µm microvia diameters, much larger than the Cu trace widths. In addition, the laser landing accuracy is about ±7 µm according to the hole positioning accuracy roadmap for laser drilling machines.[6] This places severe limitations in scaling to less than 40 µm I/O pitch RDL in minimum number of metal layers. Kyocera demonstrated the best combination of vias, pads and routing lines for panel organic interposers, Advanced Package X (APX) [7], using conventional panel scale SAP technology with 50 µm bump pitch, 20 µm vias, 32 µm capture pads, and 6 µm lines and spaces. The gap between two adjacent pads is 18 µm, which allows one Cu trace to escape in the 50 µm bump pitch region. A typical fine pitch SAP configuration is shown in Fig. 1. The reduction of microvia diameters and associated pad dimensions will allow the design engineers to use a finer pitch. In order to reduce via diameters, photolithography has been used to form ultra-small microvias. Shinko demonstrated 10 µm diameter microvias at 40 µm pitch using a spin-on 5 µm thick liquid photosensitive dielectric on standard high-density

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interconnect (HDI) layers for 2.1D organic interposers called i-THOP. [8] In this research, 100 µm thin glass panels were used as the core and 5 µm thick dry film photosensitive dielectric, IF4605, was used for both trench and microvia layers.

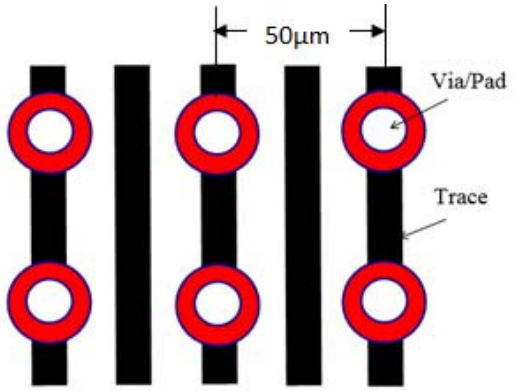

Figure 1. Typical fine pitch RDL via-in-pad routing configuration on panel organic interposer by SAP with one wire in a 50um pitch

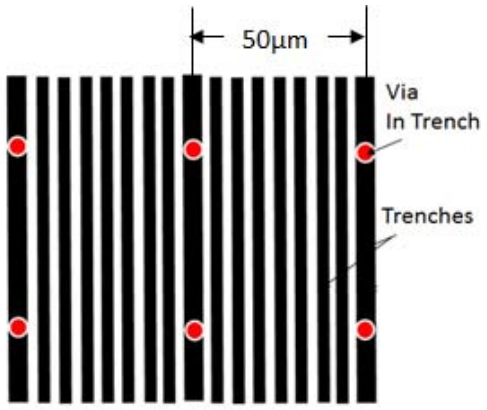

Figure 2. New type RDL via-in-trench routing configuration on panel glass by Photo Embedded Trench approach with about 10X increment of wiring capability compared to figure 1.

The smallest microvia diameter demonstrated using the dry film was 2 µm. In such a lithographic process, all the vias were transferred from a pattern on a mask to the RDL layer simultaneously so that their relative positions are fixed. The precise via position with the photolithographic tool in addition to the excellent dimensional stability of glass allows the use of smaller capture pads or to design pad-less vias. The vias were fully filled with copper and the trenches were formed on top of these solid Cu vias. Thus, a new type of via-in-trench structure was formed. Fig. 2 shows the via-in-trench configuration without using any capture pads. By comparing Fig. 1 and Fig. 2, one can see that the new type via-in-trench has much higher routing capacity. In the case of 2 µm padless vias with 2 µm lines and spaces, 10 or more copper traces can escape from a certain fixed pitch resulting in 10X wiring capability increment, with 3 to 4 escapes for a 20 µm bump pitch. Table 1 summarizes the current state-of-the-art interposer RDL technologies, compared to the glass interposer RDL described in this paper.

TABLE 1. STATE-OF-THE-ART INTERPOSER RDL TECHNOLOGIES

	Organic Interposer	2.1D Interposer	Silicon Interpose	SWIFT	Glass Interposer
Pitch, µm	50	40	45	30-50	20
L/S, µm	6	2	0.4	2	2
Via, µm	20	10	~1	n/a	2
Patterning	DFR*	LPR**	LPR	LPR	DPD***
Process	SAP	SAP + BEOL	TSV + BEOL	BEOL	Embedded Trench
Platform	Panel, Organic	Panel, Organic	Silicon, TSV	Wafer, Si-less	Panel, Glass
Institute	Kyocera	Shinko	Xilinx	Amkor	GIT/PRC

Note: *Dry Film Photo Resist, **Liquid Photo Resist, ***Dry Film Photo Dielectric,

II. PHOTOLITHOGRAPHY AND FINE CIRCUIT STRUCTURE PATTERNING IN PHOTOSENSITIVE DIELECTRICS

Photolithography has been the most widely used process in semiconductor and package industry for fine circuitry structures patterning. It has the best capability of producing high quality structures with the most precise definition in research, development and mass production at low cost. In most cases including SAP, it is used to transfer the designed patterns from a mask onto the surface of a dielectric layer through a photo resist. The photo resist is used as a temporary material for pattern transfer and metallization. After circuit patterns are metallized, the photo resist will be stripped away. In the photo trench approach, photolithography is used to transfer the designed patterns from a mask directly on to the dielectric material. No photo resist is required, therefore, some of the associated processes such as photo resist lamination and stripping are eliminated. The photo trench approach has advantages of making precision structures from sub-micron to hundred micron features depending on the resolution of the photolithographic tools and photosensitive dielectric materials.

The advantages of photolithography used here are: 1) creating very fine structures including trenches and vias, 2) parallel process with all trenches or all vias created simultaneously, and 3) precise registration. All the trenches and vias are formed precisely according to the mask design which is a big concern for UV laser patterning. An advanced projection stepper, UX-44101 from Ushio Inc., installed at Georgia Tech PRC was used for fine line and

small via photolithography. This tool is equipped with a high power i-line (λ = 365nm) light source and has a 2 µm resolution in a 100 mm diameter or 70mm x 70mm large-panel exposure area. The alignment accuracy is ±1 µm. The tool has ± 10 µm depth of focus (DOF) to accommodate for substrate warpage and thickness non-uniformity. Test results showed that minimum critical dimension (CD) achieved was 1.5 µm line and space and 2 µm diameter vias. Fig. 3 shows micrograph of 1.5 to 4.5 µm comb structure photo trenches with depth of ~5 µm in liquid photosensitive dielectric PN-0371D.

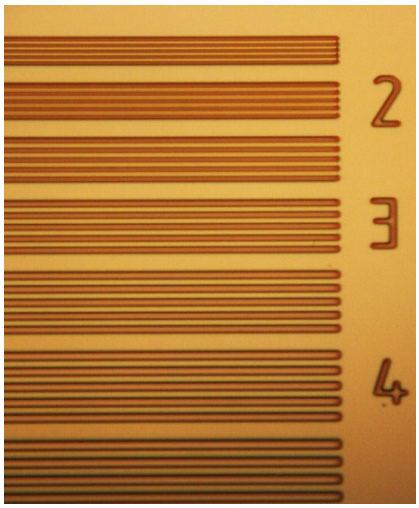

Figure 3. Micrograph of 1.5 to 4.5 µm comb structure photo trenches fabricated on thin glass panel using ~5 µm thick liquid polymer dielectric PN-0371D film

III. Photo Trench Embedding Technology vs. Semi-Additive Process

The technology used for high density wiring substrate for flip chip BGA is sequential microvia build-up technology based on SAP which was developed at IBM Japan in 1980s.[9] This technology in 2014 demonstrated its feasibility of 50 µm pitch and 6 µm line and space [7]. Future fine pitch single chip packages, 2.5D interposers and high density fan-out WLP require routing line widths to scale down to 1-2 µm. Challenges associated with the electroless Cu seed panel- based SAP process to achieve 1-2 µm feature sizes include: 1) rough surface due to the desmear of the polymer dielectric to achieve sufficient adhesion of copper to polymer; 2) seed layer etching in narrow spaces causing damage to the copper traces; 3) fine traces delamination due to insufficient bonding forces; 4) Palladium residues in ultra-small gaps causing electrical leakage; 5) height non-uniformity after Cu electroplating; and 6) thin dielectric film lamination and non-planar surfaces for multi-layer RDL. Considering these challenges, there is a perceived limit of 5µm Cu trace width for today's SAP processes.

The photo embedded trench process has advantages over the conventional SAP. It enhances the adhesion reliability of fine traces by embedding them into the dielectric layer and eliminates the seed layer etching which are the two biggest challenges for SAP technology. Fig. 4 shows the images of raised 1.5 µm fine walls (left) and 1.5 µm fine trenches (right). The raised structures were collapsed, while the embedded trenches were stable. Both of them were in the same sample and closer each other.

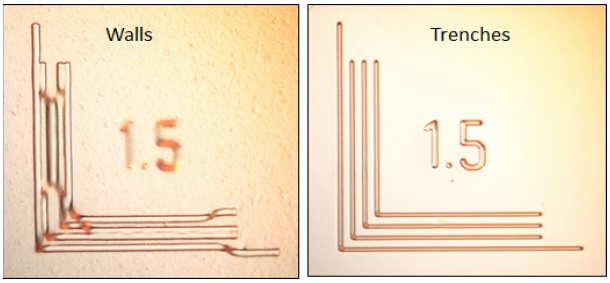

Figure 4. 1.5 µm wide raised structure (wall) collapsed (left), 1.5 µm embedded trenches stable (right).

In summary, Fig. 5 shows the configurations and challenges in traditional SAP structures: fine trace collapsed or lift-off during the seed layer etching, seed layer residue, copper height variations and so on. In contrast to SAP, Fig. 6 shows the configuration of embedded trench approach. All the traces are embedded in the polymer layer so that they are reliable, including very fine traces, in terms of adhesion and electrochemical migration because of the Ti barrier. There is no conductive seed layer beneath the traces. There is no seed layer needed to be etched away. Instead, there is an extra copper layer on the top of the surface. This layer of copper has to be removed. From the figure, one can also see that the surface of copper traces is flat.

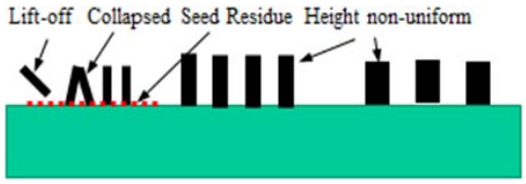

Figure 5. Traces raised on dielectric layer surface with seed layer etching difficulties, plated copper height non-uniform and face trace damages.

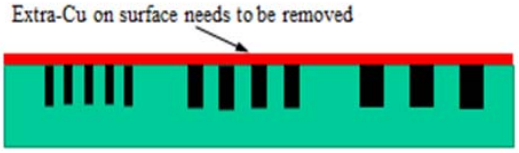

Figure 6. Embedded trenches: traces buried in dielectric layer and protected. Surfact flat, no seed layer etching required. Extra copper on surface removing is needed.

IV. New Generation Photosensitive dielectric materials

The key materials used in the photo trench approach are ultra-thin (5 µm) photosensitive dry film dielectric polymer IF4605 by Tokyo Ohka Kogyo Co., Ltd (TOK) and thin glass panel core substrates provided by Corning and Asahi glass companies. The film IF4605 is a negative toned material which is a standard three layer structure similar to the dry film photo resist. It is sensitive to wavelength of 365 nm i-line. Its dielectric constant is 3.8, glass transition temperature is 250^0C and coefficient of thermal expansion is 45 ppm/K. Vacuum laminator was used for laminating the film to the substrate. Lamination temperature used was 90^0C and cure temperature was 200^0C. Table 2 lists the key process conditions for IF4605. In addition, liquid PN-0371D was also tested. It is a positive toned material. The PN-0371D was spin on to the substrate. The thickness of liquid film can be in the range of 2-6 µm at a controlled spin rate. The 1.5 µm finest trench was achieved in ~5 µm thick PN-0371D liquid film shown in Fig. 3.

TABLE 2. Key Process Conditions of IF4605

Process	Equipment	Conditions
Lamination	Vacuum Laminator	90°C, 30 sec.
Exposure	Ushio UX-44101	600 mJ/cm2
Post Bake	Oven	90°C, 20 min.
Development	Immersion, PGMEA	90 sec.
Cure	Oven	200°C, 1 hour
Seed layer	PVD Cu/Ti	200nm/25nm
Metallization	Electrolytic Plating	Cu filling

V. Methods of Microvia Formation and Ultra-small Photo Vias

A. *Methods of Microvia Formation*

There are three primary methods used in package substrate fabrication for microvia formation. They are photo-definable, plasma etch and laser ablation. Photo-definable via was the first technology used to make microvia that initiated the high density interconnect (HDI) substrate for flip chip applications in the 1980-1990's.[9] The process flow is similar to solder resist patterning by photolithography. All vias, as per the mask design, are formed at the same time in the photo-defined via formation method. The minimum thickness of old generation photosensitive dry film material we used was 25 µm. The minimum diameter achieved was 25µm on the 25 µm thick film [10]. This method was limited by material availability. Later, laser ablation dominated the via making process for package substrates in 2000s' due to the rapid development of high speed CO_2 lasers. CO_2 lasers emit infrared light with wavelengths between 9.3 µm to 10.6 µm. The mechanism of CO_2 laser ablation is based on photo thermal ablation by burning the polymer material away from the desired areas to form vias. The relative long wavelength limits the minimal focus diameter of the laser beam. Apart from thermal effects, the via diameter size drilled by CO_2 laser is limited, and is in the range of 40-60 µm. UV laser has shorter wavelengths of 355 nm and 266 nm. The mechanism of UV laser ablation is based on a combination of photo chemical and thermal ablation. The UV laser beam can be focused to a small spot with high power density. These beams can break molecular bonds and ablate most of the dielectric polymers and metals, such as copper, nickel and gold. The via diameter formed by UV laser is about 20 µm mentioned before.[7] The laser via formation is a point-to-point drilling process. It is time consuming and non-cost effective for a very large number of vias. The via registration uncertainty requires large pads for via landing that limits the via pitch reduction. Plasma etching, similar to the photo-defined vias process, is a mass via formation. But it is difficult to make small vias due to its nature of isotropic ablation. Lateral etch beneath the mask will occur.

B. *New Generation Photovias*

As discussed above, it is important to explore alternative ways to reduce via size and improve via registration accuracy to achieve finer via pitches. Excimer laser using shorter wavelengths has the ability to create via diameter of 8 µm vias in build-up dielectric layers. [11] This technology is now in the research and development phase collaborated by PRC and Suss MicroTech. Liquid photosensitive polymer was used to create 10 µm diameter vias in spin-on 5µm thick film for Shinko's 2.1D interposer. It appears that photo definable vias are coming back after 20 years. With the development of new generation ultra-thin dry film photosensitive dielectrics at TOK, we have demonstrated microvia diameter scale down to 2 to 5 µm with a pitch size of 1 to 1. Fig. 7 shows micrograph of 2 to 5µm diameter area array microvias formed in a dry film photosensitive dielectric film IF4605. The minimum via pitch demonstrated here is 4 µm. Again, the thickness of the film is 5 µm. So the aspect ratio is 2.5

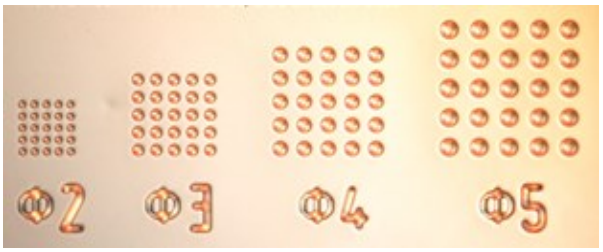

Figure 7. Micrograph of 2 to 5µm microvias formed in 5 µm thick photosensitive dry film IF4605. The minimum via diameter opened was 2 µm at 4 µm pitch

VI. Test Structure and Fabrication Processes Flow

A. Design of Test Structures

There were two sets of masks used in this study. The first set was designed for process development and optimization. The mask consists of 1.5 to 5 µm fine line and space comb structures along with 2 to 5 µm small vias. Feasibility studies on trenches and vias can be accomplished at the same time by using one mask. The mask was designed for both negative tone and positive tone which is suitable for both IF4605 and PN-0371D. The second set was designed for trench and via integration test. There were two masks designed and plotted for the second set. One was designed exclusively for trench study. Another one was for vias only. Fig. 8 is a test coupon image on a glass mask which includes six test structures: The pitch is 20 µm for all the six structures. The line and space for top three structures is 2.5 µm. There were 3 µm line and space and 5 µm lines for the bottom three structures. The 3 µm features were for routing and the 5 µm wide feathers were designed to capture vias within the trenches for a padless multi-layer RDL structure.

B. Process Flow

The major process steps of embedded trench approach for 2.5D interposer and fan-out-RDL include: 1) IF4605 film lamination, 2) photolithography (UV exposure, post exposure bake and development), 3) metallization including PVD conductive seed layer and electrolytic copper plating, and 4) etch back of the excess Cu on the dielectric surface. A thin panel glass was used as the core substrate. Glass has excellent electrical and mechanical properties. It's flat surface and excellent dimensional stability is great for fine feature photolithography and precise registration that are critical for ultra-high wiring density interposers and fan-out packages. For 2.5D interposer, the IF4605 is laminated as the first dielectric layer on a conventional build-up layer on glass core. Fan-out processes require IF4605 lamination over the surface of embedded, reconfigurable dies on a carrier. Micro-vias are then formed in the dielectric layer. For fan-out structures, these vias provide a chip-to-package interconnect. As via layer process is completed, a subsequent IF4605 lamination is performed to serve as a trench layer. These trenches are metallized using the same process as the previously formed photo-vias. This process is called dual-layer-photo-trench process. Trenches, vias, and pads have different dimensions which have to be completely copper filled. Copper plating is a big challenge for filling these structures with largely different aspect ratios. The dual-layer process will reduce the copper plating challenge. Fig. 9 shows the process steps for photo trench fabrication on thin glass as well as for photo via fabrication.

VII. Test Results and Discussions

A. Embedded Photo Trenches

The resolution of both dry film and liquid film was tested for photo trench formation. In photolithography, the amount of UV dose, post exposure bake and the focus of the UV beam are critical. With optimization of process conditions, the minimum trench size obtained was 2 µm in dry film IF4605 and 1.5 µm in liquid based film PN-0371D. Fig. 10 shows cross section of photo trenches formed in PN-0371D filled with plated copper and after surface copper etched (Step 6 in Fig. 9). The width and space of the trenches ranges from 1.5 to 5 µm (left to right with an increment of 0.5 µm). From the cross section, one can see that the embedded traces have an excellent shape with flat top and fixed bottom surfaces. The flat surface will be critical during photolithography for fabrication of fine structures in the immediate next metal layer. The height of the trenches measured in Fig. 10 is 4.8 µm. Thus, the trench aspect ratio demonstrated is 3.2.

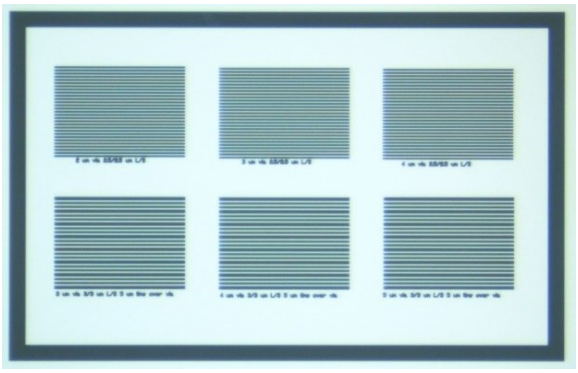

Figure 8. Via-in-line test coupon for exploring routing capability of embedded photo trenches and photovias. The line and space for top 3 structures is 2.5 µm and for bottom 3 structures is 3um.

B. Photo Vias

Similar to the photo trench studies, both dry film IF4605 and liquid PN-0371D were tested for the minimum via diameter that can be obtained with optimization of UV dose and UV beam focus. Test results showed that minimum diameter of 2 µm vias could be achieved in both materials. A 25nm Ti and 200nm Cu conductive layer by PDV sputtering was used as seed layer. After copper plating and copper filled in the trenches, Step 6) chemical spray etching and microetching (Step 7 and Step 8) were performed to remove extra copper on surface. Fig. 11 (left) shows top view of 2 µm and 3 µm diameter vias in PN-0371D after surface copper fully removed. Fig. 11 (right) shows the cross section of a row of 3 µm vias.

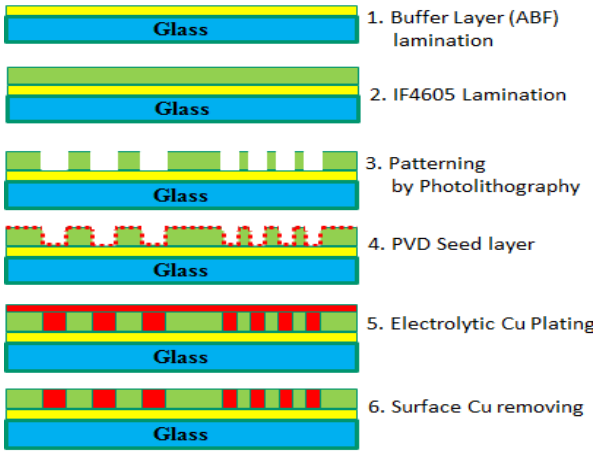

Figure 9. Photo Trench (or Photo Via) Fabrication process steps.

Figure 10. Cross-sections of embedded 1.5 to 5 µm copperm traces in PN-0371D dielectric after surface copper etching and completed embedded traces with flat copper surface. The height of the traces is 4.8 µm and thus the trench aspect ratio is 3.2

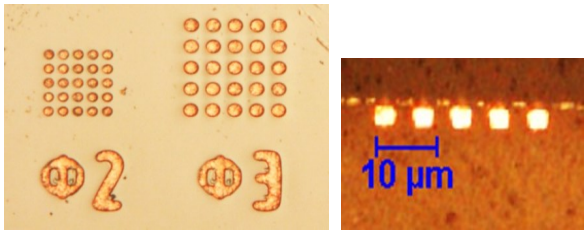

Figure 11. Top view of 2 and 3µm vias after Cu plating and surface copper etching (left) and cross section of a row of 3 µm vias (right).

C Integration of Photo Trenches and Photovias

A 100 µm thick glass was used as core substrate for the integration of photo trenches and photo vias. The panel sizes used were 6"x 6" and 4"x4". The glass surface was first cleaned and coated with a silane chemical. ABF GX-92 (15 µm) films were laminated on both sides of the glass. For simplification in the sample fabrication process, instead of using the PVD Ti-Cu seed layer, a 1.5 µm thick copper foil was laminated on ABF GX-92 film (both sides). Subsequently, IF4605 dry film was laminated on the Cu foil of the sample (both sides) and vias were formed using photolithography. Bottom up plating was performed to fully fill copper in the vias. The next step was lamination of a second layer IF4605 film on top of the via metal layer. Trenches are formed in this second layer IF film by photolithography. Precise alignment was performed for via and trench integration. After the trench process is completed, Fig. 12 shows top view of the entire fabricated coupon with six trench structures and microvias. The microvias can be seen in trenches in the six structures. They were aligned well with relative trenches. The via diameters are: 2 µm (top left), 3 µm (top middle and bottom left), 4 µm (top right and bottom middle) and 5 µm (bottom right). The via pitch of all the structures is 20 µm.

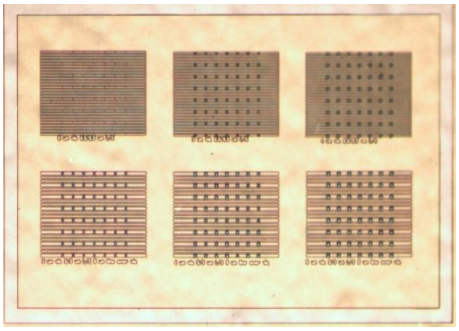

Figure 12. Fabricated test coupon with 6 structures consisting of embedded fine trenches integrated with small microvias on 100 µm thick glass core with good alignment; via pitch for all is 20 µm, min. via is 2 µm.

Fig. 13 shows the zoomed-in top view of the structure at bottom left with 3 µm vias and 3 µm trenches. The trench width for via interconnection is 5 µm. There are two trenches in a 20 µm pitch. Total routing wires is three per pitch. The configuration of the new type RDL is L/S/Via/T = 3/3/3/5 µm with 20 µm via-to-via pitch. Fig. 14 shows the zoomed-in view of the structure at top-left which has the smallest vias and finest trenches in the design. The via diameter is 2 µm, the trench width is 2.5 µm. The trench width for via interconnection is 2.5 µm as well. There are three trenches in a pitch. Total routing wires is four per pitch. The configuration of the RDL is L/S/Via/T = 2.5/2.5/2/2.5. Comparing with traditional configuration of SAP based RDL, the new generation RDL has much higher wiring density capability.

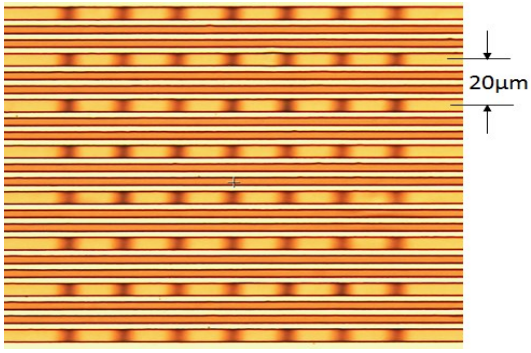

Figure 13. Zoomed in view of embedded fine trenches integrated with small microvias on 100µm glass. Trench width and space are 3µm each, microvia diameter is 3µm, and trench width for via interconnection is 5µm. The configuration of the new RDL is L/S/Via/T =3/3/3/5 µm.

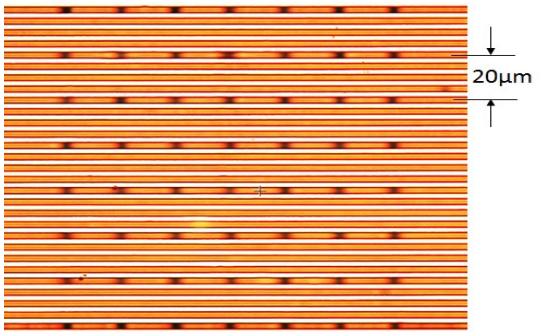

Figure 14. Zoomed in view of embedded fine trenches integrated with small microvias in IF4605 dry film using 100µm thick glass core. Trench width and space are 2.5µm each, microvia diameter is 2µm and trench width for via interconnection is 2.5µm. The configuration of the RDL is L/S/Via/T = 2.5/2.5/2/2.5 µm

SUMMARY

The semiconductor feature size down to 14nm node and copper pillar technology development drive the IC bump pitch down to 40µm and below. Today's sequential build-up panel-based technology based on SAP is facing its limits for fine pitch requirement. Laser embedded trench approach overcomes the challenges of SAP. However, issues of resolution, depth control, positioning accuracy and time consuming still remain in the laser ablation process for trench formation. Photo embedded trench associated with photo via approach is developed due to extremely high resolution, controlled trench depth and high precision in registering the fine features at exact locations. In contrast to laser ablation using point-to-point serial drilling process, photo trench approach uses parallel photolithographic process. The RDL stack made by photo trench process has the following advantages: 1) integration of small diameter vias with uniform depth fine trenches using existing photolithography tools; 2) panel scalable and low cost; 3) eliminates the seed layer etching process to form finer lines and spaces; 4) reliable adhesion of fine traces due to embedding in the dielectric layer; and 5) planar surface for multilayer integration. This work pioneers the demonstration of new generation RDL via-in-line configuration with 2 µm diameter ultra-small vias and 2.5 µm wide trenches in dry photo dielectric film for panel level package RDL technology. This new generation RDL technology can be used for 2.5D interposers and high-density fan-out packages at both wafer and panel level with high routing capability at low cost.

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