# *Effect of Ultra-Fine Pitch RDL Process Variations on the Electrical Performance of 2.5D Glass Interposers up to 110 GHz*

Chandrasekharan Nair, Hao Lu, Kadappan Panayappan, Fuhan Liu, Venky Sundaram, Rao Tummala
3D Systems Packaging Research Center, 813 Ferst Drive, Georgia Institute of Technology, Atlanta, GA, USA
Email: cnair3@gatech.edu

*Abstract*

**This paper discusses the effect of process induced variations in copper transmission lines on their electrical performance up to 110 GHz, fabricated by semi-additive processes (SAP) for redistribution layers (RDL). The motivation of this research is to quantify the effect of the process variations in RDL traces by SAP, thus enabling electrical designers to reduce design iterations to achieve precise impedance control. The paper will primarily discuss results from analytical electromagnetic (EM) modeling, full-wave EM modeling and initial frequency domain characterization. The escalating demand for high bandwidth electronics, has driven the adoption of wide bus interconnections between logic and memory ICs. Wireless communication protocols in smartphones, automotive and IoT systems also require high frequency signal transmission (60-100 GHz) in the near future. Both the high speed and high frequency signals impose major challenges, in precise circuit definition, in addition to the low cost and low power consumption constraints. At such fine feature sizes, any imperfections in the SAP technology, such as surface roughness of polymer dielectrics, tapered cross sections of the traces and tapered microvias in polymer dielectrics, impact the impedance and signal loss, and these effects need to be quantified electrically. This paper presents modeling research to understand the effect of different process induced variations on electrical performance of transmission lines on glass interposers, correlated with the measured data in published literature.**

**Keywords-Component, Computational electromagnetics, RDL, SAP, 2.5D interposers**

## I. INTRODUCTION

Wireless and wired communication systems are driving the demand for high bandwidth, in such applications as high definition video streaming, autonomous driving and image processing.. There is an increasing trend towards integrating logic, memory and RF ICs on a single interposer package. The automotive industry is moving towards the 77 GHz frequency band for highly intelligent Adaptive Cruise Control (ACC) and Collision Avoidance Systems. [1] The most recent product MRR1Plus 77GHz automotive radar from Bosch integrates two radar dies (transceiver and receiver components) in a single fan out wafer level package developed by Infineon.[2] Wireless HDTV is yet another promising application for 60 GHz frequency band to achieve the required high data rates.[1]

The challenge today is to develop these systems into highly integrated, low cost and low power consuming wireless devices. One of the approaches to develop such a system is to use large panel scalable interposers for very high performance systems and while for the mobile devices, use the panel scalable fan out packages.

For such panel scalable fabrications, glass serves as a promising candidate for the core material due to its excellent electrical properties for high end mm-wave systems, exceptionally smooth, flat surface, low moisture absorption and high dimensional stability for high precision lithography.

Panel scale RDL with glass or laminate cores is currently achieved by what is known as semi-additive process (SAP). The SAP technology for high density RDL with 6 µm wide Cu traces have been demonstrated using electroless Cu seed deposition process on a dry film epoxy dielectric for a panel scale organic interposer APX by Kyocera.[3] Similarly, SAP was used to demonstrate i-THOP by Shinko with 2 µm Cu traces with PVD Ti-Cu seed on a liquid based spin-on photodielectric.[4] At fine feature sizes, the imperfections in SAP technology such as surface roughness of polymer dielectrics, tapered cross sections of the traces (after seed layer etching process) and tapered microvias (laser drilled) in polymer dielectrics need a thorough analysis to electrically qualify them at high frequencies. In an attempt to address such a need, this paper first identifies the resulting tolerances with SAP technology. It then presents the effect of different RDL process variations on system performance through 3D EM modeling up to 110 GHz and few characterizations up to 20 GHz. Three different transmission line geometries namely, microstrip line, stripline and coplanar waveguide (CPW) were analyzed. Single ended signaling were considered for all the three transmission line geometries. The imperfections in terms of tapered cross section and tapered microvias were analyzed up to 110 GHz using the Ansoft HFSS full wave solver. The copper to polymer interface roughness was modeled by using ADS through experimentally measured surface roughness.

In summary, the paper identifies the resulting tolerances with SAP technology and reports the effect of process variations on electrical performance for different frequencies up to 110 GHz through modeling. It also indicates the design guidelines for the three commonly used transmission geometries by identifying the frequencies at which the process variations start to significantly affect the electrical performance of the system.

## II. SEMI-ADDITIVE PROCESS (SAP) FLOW

The conventional semi-additive process flow for a panel substrate is shown in Figure 1. [5] Once the Cu is patterned on the core material (glass or laminate core), a thin dry film polymer dielectric is laminated on both sides of the core followed by its curing. Laser microvias are drilled in the polymer dielectric. The major laser systems used today for this purpose are UV/$CO_2$ lasers and it can drill microvias in the range of 20-100 µm via diameters. Excimer lasers have been

shown to drill microvias as small as 8-10 µm in diameter, in a 10 µm thick polymer dielectrics. The laser drilled microvias are generally tapered in shape. Figure 2 shows a 50 µm microvia drilled in 15 µm thick epoxy dielectric dry film using UV laser.

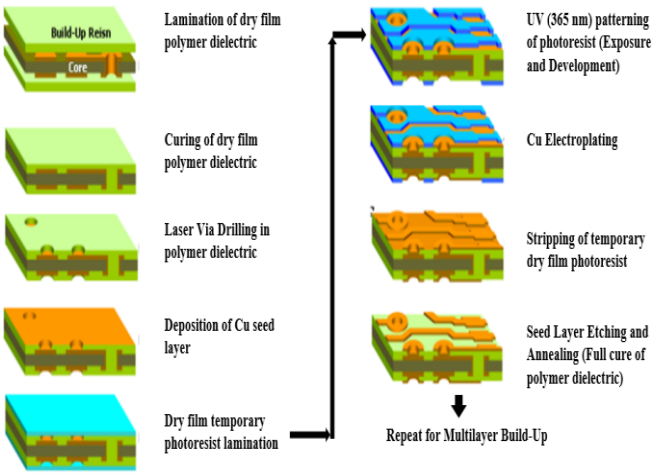



Fig 1. Semi-Additive Process Flow [5]

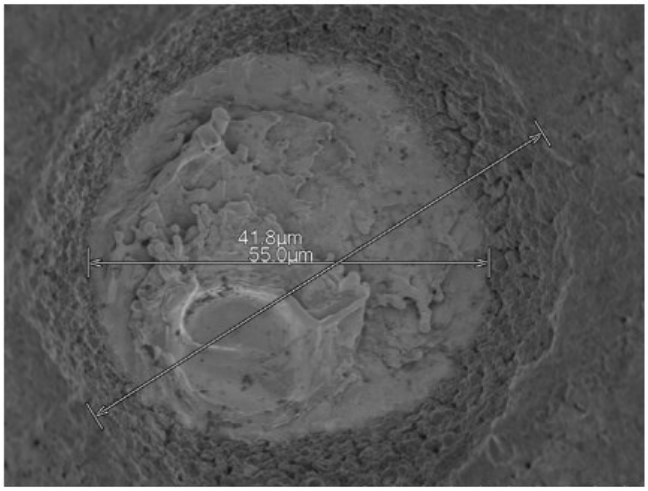
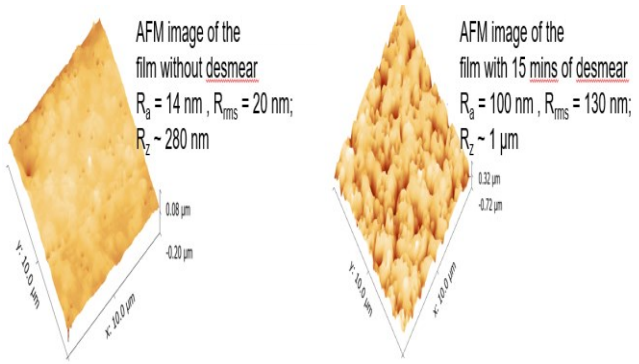



Fig 2. UV laser drilled microvia with the taper after the chemical desmear step to clean the via residues

The next step is the Cu seed layer deposition in the via drilled polymer dielectrics. This can be achieved today using two techniques, namely: (a) Electroless Cu seed and (b) Sputtered Ti-Cu seed. Electroless Cu seed process is widely used as it enables simultaneous double-side deposition and is also a high throughput process. In the case of electroless Cu seed technology, the polymer dielectric surface is first roughened (desmeared) using a wet etch permanganate solution in order to enhance the adhesion. Then, electroless Cu seed is deposited by a wet solution process using palladium particles as catalysts. The basic mechanism of Cu adhesion to the polymer dielectric here is a combination of mechanical interlocking and chemical adhesion of Pd catalysts to polymer. Typical electroless Cu seed thickness ranges from 300-500 nm. The roughness profile of an advanced epoxy dielectric film with no desmear treatment and after desmear treatment for electroless Cu seed deposition is shown in Fig 3 (measured by Atomic Force Microscopy(AFM)). In Fig 3, $R_a$ stands for the average roughness, $R_{rms}$ for the root mean square roughness and $R_z$ for the average distance between the highest peak and the lowest valley measured within five sampling lengths on the dielectric surface.




(a) (b)

Fig 3. Roughness profile of an epoxy dry film dielectric (a) No desmear treatment (b) After 15 mins of desmear treatment

The next steps in the SAP process flow are UV photolithography using dry film photoresist to pattern the desired circuit followed by Cu electroplating in the opened areas. Most dry film photoresists used for panel scale packages are of negative type. Once the temporary photoresist is stripped off after the Cu plating process, the most critical step, namely, etching of seed layer is performed. This step decides the final dimensions of the patterned Cu traces.

## III. SEMI-ADDITIVE PROCESS VARIATIONS

A summary of the semi-additive process is discussed above. Based on this discussion, three main critical variations in SAP are chosen to study their effects on the electrical performance of RDL stack for different frequencies up to 110 GHz. These three variations are: (A) Tapered Cu traces with narrower widths than desired as per the design (B) Tapered Microvias (C) Surface Roughness of the polymer dielectric

### *III A. Tapered Cu traces with narrower widths*

The Cu traces are the most critical features in high performance systems like 2.5D interposers. The structure of these Cu traces decide the speed and performance of the communication between digital dies. With panel-scale SAP, the most common used photoresists are dry-film based and dry film imaging generally results in tapered patterns. After Cu electroplating is performed on these patterns, the conductive seed layer etch step in SAP decides the final Cu trace dimension. The current state of the art electroless Cu seed is considered here, where Cu seed and Pd residues need to be etched. Both Cu and Pd etchants not only etch the copper seed layer, but also etch the electroplated copper patterns to a certain extent. This results in narrower copper lines than that of the original design. Fig 4 shows the effect of polymer surface roughness on the narrowing of plated fine Cu traces.

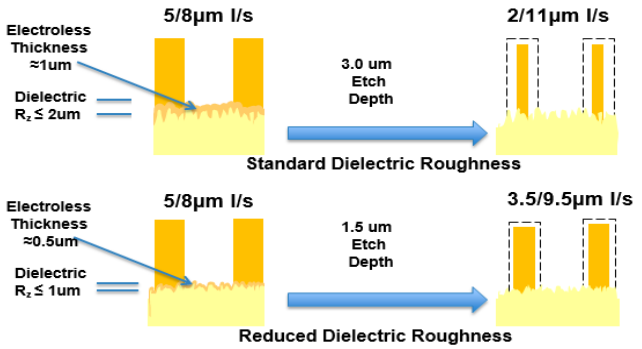



Fig 4. Schematic showing narrowing of plated Cu patterns after conductive seed layer etching process [Courtesy: Atotech]

As an example for experimental result, we have referred here to a 20 µm Cu trace fabricated using SAP. A typical profile of the 20 µm Cu trace after seed layer Cu etch and Pd residue etch is shown in Fig 5. [6], [7]

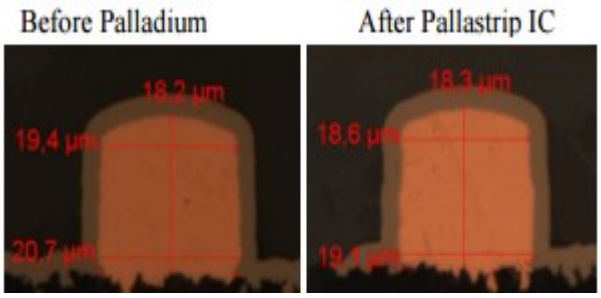



Fig 5: 20 µm Cu trace profile after seed etch (Cu and Pd); Pallastrip IC® is an Atotech Product [6],[7]

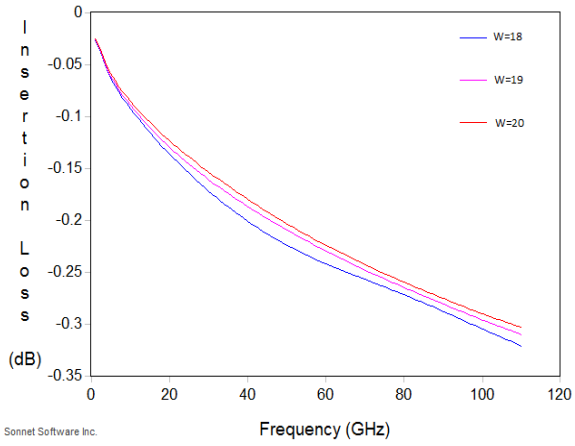
For simulations, the 3D models of microstrip line, stripline, and CPW were analyzed in HFSS with wave ports, to study the performance impact of change in line widths due to fabrication processes. For all models, the polymer dielectric assumed here is a low loss advanced epoxy polymer dry film dielectric ABF GY-11. The thickness of polymer dielectric (ABF-GY11) was assumed to be 15 µm. The properties of ABF-GY11 are summarized in Table 2. One important simplification in simulating all the models in this paper is that the frequency dependency options of dielectric properties for the polymer dielectric film have been set to piecewise linear input by default as per the HFSS software. This might not be well in accordance with the actual dielectric behavior of the polymer at very high frequencies. Hence, the insertion loss values at high frequencies should not be considered as absolute values and hence, are used as relative measures to understand the effect of different process variations. According to the SAP process flow, the distance between copper layers is approximated to be polymer thickness minus the deposited copper thickness. The copper thickness in this study was assumed to be 5 µm. Therefore, in the microstrip line and stripline models, the distance between ground layer and signal layer is 10 µm. In the case of CPW, which is a single metal layer structure, the 15 µm thick ABF and the glass substrate beneath the ABF acts as the dielectric layer. All the three types of transmission line models were designed to achieve 50 ohms characteristic impedance. The calculated design parameters are listed in Table 1. All these parameters were calculated are using a 2D transmission line model. The simulation results from Ansoft HFSS for these designs with different line widths are shown in Figure 6. The effective transmission line length after de-embedding is 1000 µm for all the three models.

Table 1. Geometric Parameters calculated for 50Ω impedance

| Microstrip | Stripline | CPW |
|---|---|---|
| Signal line width (µm) | Signal line width (µm) | Signal line width (µm) |
| | | 15 |
| 20 | 7.5 | Signal to ground gap (µm) |
| | | 4.35 |
| Dielectric thickness (signal to ground) (µm) | Dielectric thickness (ground to ground) (µm) | Dielectric thickness (µm) |
| 10 | 25 | 15 |

Table 2. Properties of the Dielectric Film GY-11

| Properties | Measurement method | ABF GY-11 |
|---|---|---|
| $T_g$ (°C) | DMA | 165 |
| CTE (ppm/°C) (25-150 °C) | Tensile TMA | 26 |
| (150-240 °C) | | 81 |
| Dielectric constant ($D_k$) | Cavity Perturbation, 5.8 GHz | 3.2 |
| Dielectric Loss Tangent ($D_f$) | Cavity Perturbation, 5.8 GHz | 0.0042 |

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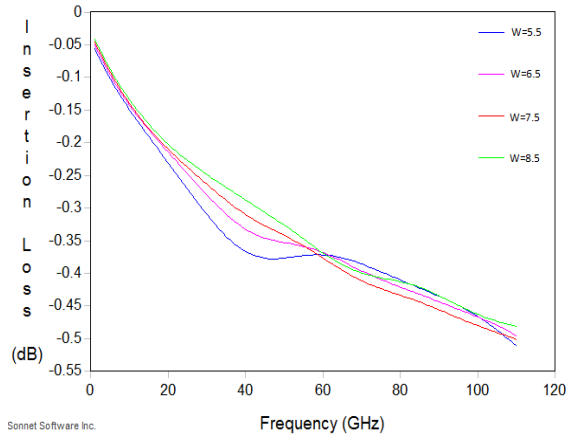


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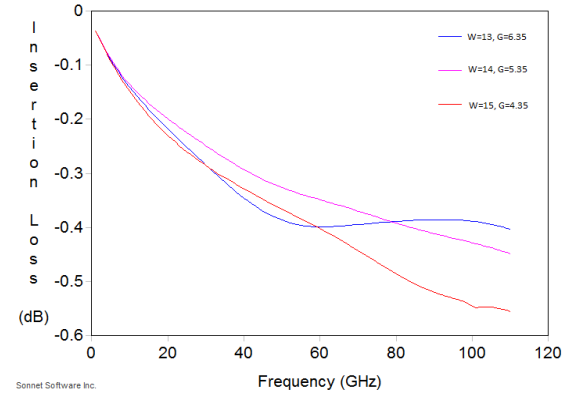



(c)

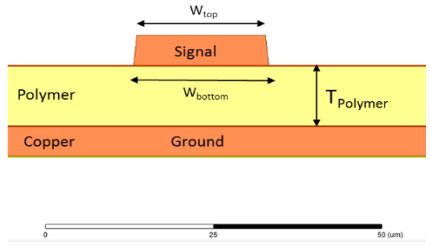
Figure 6. Insertion losses for (a) microstrip line, (b) stripline, and (c) CPW from Ansoft HFSS simulations, where W is signal line width in µm, and G is the gap between the signal to ground in µm, for the case of CPW.

For microstrip lines, the designed line width is 20 µm. If the width is shrunk to 19 µm or 18 µm, the insertion loss increases slightly. For stripline configuration, the calculated line width is 7.5 µm. However, the insertion loss is lower below 60 GHz when the line width is 8.5 µm. It can be concluded that 8.5 µm width stripline has better performance than estimated parameters, and any width shrinkage due to process variation will result in performance loss. Similarly for CPW, the optimal parameters are w=14 µm and gap=5.35 µm, and the process variations affect the performance in a negative way.

The trapezoidal cross section of the Cu traces, as discussed above, can occur due to the dry film photoresist imaging and due to side etching of Cu traces during the seed layer etch process. This effect was also modeled in Ansoft HFSS, as shown in Figure 7. The bottom width and gaps of the three types of transmission lines were fixed to be the optimal value we got from the above line width study. The top widths and spaces between the traces were tuned to study the performance impact. The simulated parameters are shown in Table 3, and the simulation results are shown in Figure 8.

Table 3. Geometric Parameters used for simulating tapered Cu traces

| Microstrip | Stripline | CPW |
|---|---|---|
| $W_{bottom}$ (µm) 20 | $W_{bottom}$ (µm) 8.5 | $W_{bottom}$ (µm) 14 |
| | | $G_{bottom}$ (µm) 5.35 |
| $W_{top}$ (µm) 18, 19, 20 | $W_{top}$ (µm) 6.5, 7, 7.5, 8, 8.5 | $W_{top}$ (µm) 11, 12, 13, 14 |
| | | $G_{bottom}$ (µm) 8.35, 7.35, 6.35, 5.35 |
| Dielectric thickness (signal to ground) (µm) | Dielectric thickness (ground to ground) (µm) | Dielectric thickness (µm) |
| 10 | 25 | 15 |

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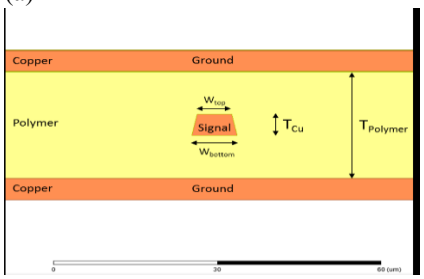


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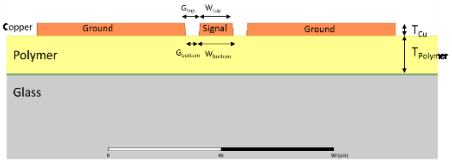
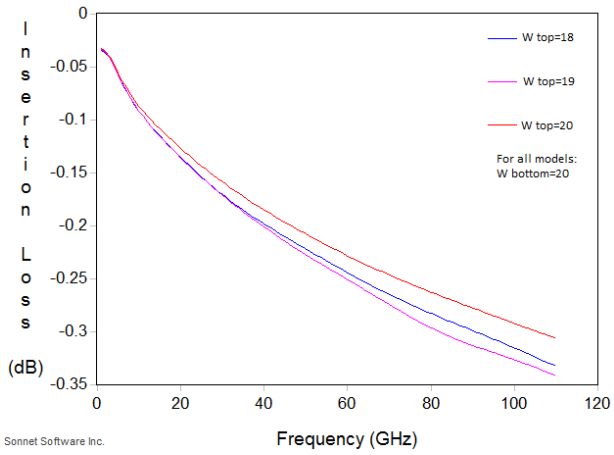
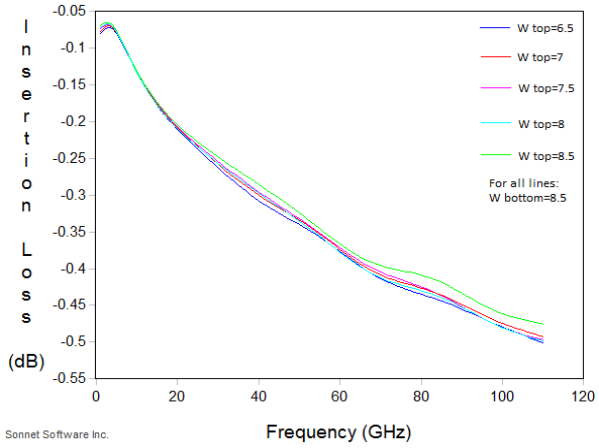



(c)

Figure 7. The trapezoidal shape model of (a) microstrip line, (b) stripline, and (c) CPW used in Ansoft HFSS.




(a)

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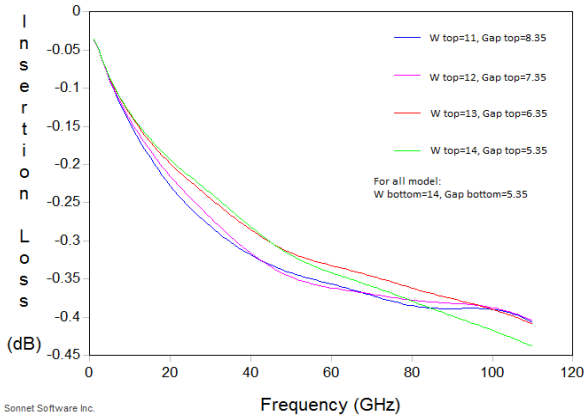


(c)

Figure 8. Insertion losses for (a) microstrip line, (b) stripline, and (c) CPW, with fixed bottom width and varying top widths from Ansoft HFSS simulations.

According to the simulation results, any change in the line shape has negative impact on the performance at frequencies above 45 GHz. For the case of CPW, a slight over-etch on the line ($W_{top}$=13 µm, $G_{top}$=6.35, $W_{bottom}$=14 µm, $G_{bottom}$=5.35) decreases the insertion loss above 45 GHz. This might be attributed to the inaccuracies in meshing. Hence, the trapezoidal cross-section of the line does affect the performance negatively, but not to a significant scale.

### *III B. Tapered laser drilled microvias*

Laser Ablation is the main technology for drilling microvias in dielectric films for panel-based SAP. The laser drilled microvias are generally tapered in shape as was shown in Figure 2. For high density RDL, excimer laser ablation technology is being studied for drilling ultra-small microvias (< 10 µm). A 10 µm top diameter excimer laser drilled microvia by Suss MicroTec Photonic Systems Inc. [8] in a 15 µm thick dry film BCB material is shown in Fig 9.

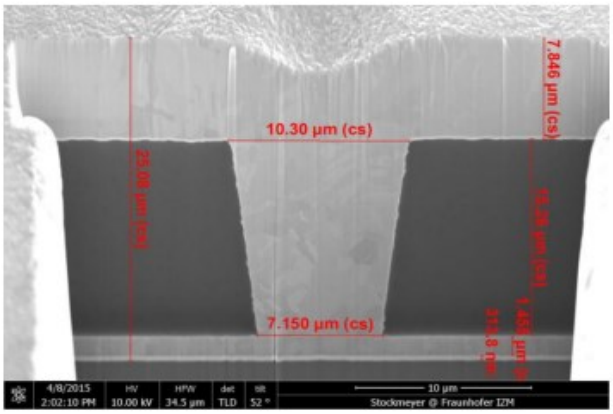


Figure 9. Excimer Laser drilled microvia (10 µm) microvia in 15 µm thick BCB dry film [8]

The effect of micro-via taper is modeled in Ansoft HFSS using microstrip line to via transitions. The cross-section of the simulated model is shown in Figure 10. The signal is inserted on the top microstrip line, and transmitted into the bottom copper layer as an embedded microstrip line. Then the signal is transmitted through another via to the top. The signal path in the model is constituted by three sections of microstrip lines (each 1 mm long) and two micro-vias. The width of two microstrip line sections on top is 20 µm while the bottom section (embedded microstrip) is 10 µm in order to match the impedance of all 3 sections to 50 Ohm. The bottom diameter of the micro-via is tuned to study the via taper effect. The simulated parameters are shown in Table 4 with results plotted in Figure 11. From the result, it can be concluded that the micro-via shape plays a negligible role for the performance of the whole transmission line structure, throughout the entire frequency range up to 110 GHz.

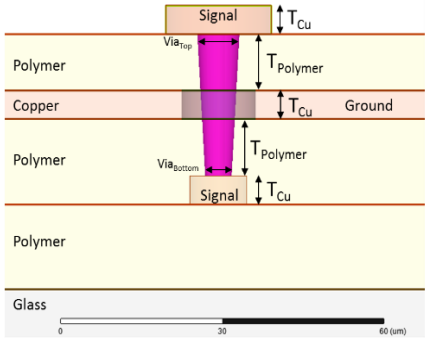


Figure 10. Microstrip line with micro-via transition model used in Ansoft HFSS simulation.

Table 4. Geometric Parameters used for Tapered Microvia Simulations

| | |
|---|---|
| $T_{Cu}$ (µm) | 5 |
| $T_{Polymer}$ (µm) | 10 |
| $Via_{Top}$ (µm) | 8 |
| $Via_{Bottom}$ (µm) | 5, 6, 7, 8 |

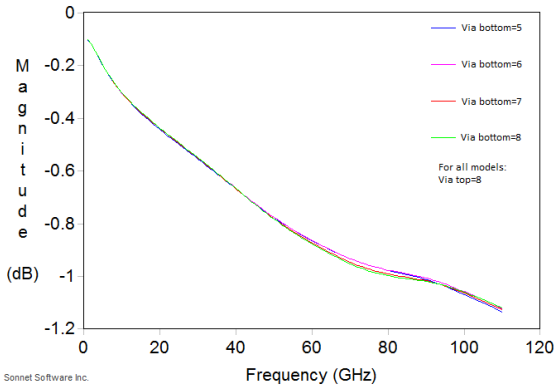


Figure 11. Insertion loss of microstrip line with micro-via transition

### *III C. Surface Roughness of Polymer Dielectric*

As discussed in Section II, the chemical wet etch desmear step before the electroless Cu seed layer deposition increases the roughness of polymer surface. This, in turn, increases the roughness of polymer-copper interface and will affect the electrical performance of fine copper traces at high frequencies due to the skin effect. A simple microstrip line model was created in ADS to study the surface roughness impact. The microstrip line was set on 10 µm thick ABF-GY11 polymer, with a signal line width of 20 µm and a length of 1 mm. The copper thickness used is 5 µm. The ABF average surface roughness ($R_a$) used in the model before and after desmear process was obtained from the AFM experimental data (Figure 3). The simulation result (Figure 12) does show that the increased interface roughness has a negative impact on the insertion loss at high frequencies. Hence, for high frequency applications, the surface roughness cannot be neglected.

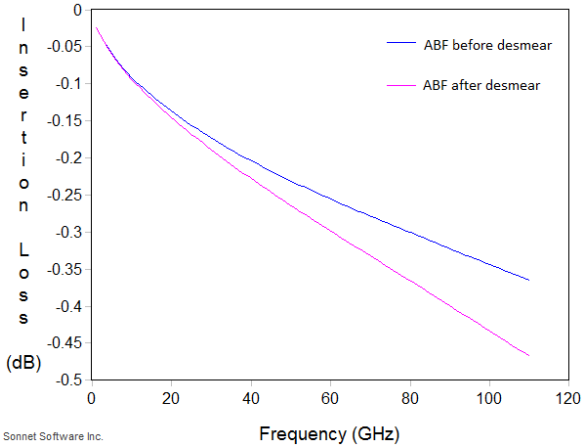


Figure 12. The simulated insertion loss of microstrip line on ABF-GY11 with different surface roughness using ADS

## IV. Summary and Conclusions

This paper identified the resulting tolerances with SAP technology and reported the effect of process variations on electrical performance for different frequencies up to 110 GHz through modeling. Three critical variations in SAP technology were identified for this study: (A) Tapered Cu traces with narrower widths than desired as per the design (B) Tapered Microvias (C) Surface Roughness of the polymer dielectric. Both narrowing and tapering of the Cu traces had undesirable effects on the insertion loss for different transmission line configurations. However, the effects were not that significant. Again, less significant effects were observed for ultra-small tapered microvias. The magnitude of the insertion loss for the transition of microstrip line with tapered microvia was significant. Surface roughness of the polymer dielectric due to wet microetch treatment of the polymer surface to improve adhesion of the electroless Cu was found to have a significant effect on the insertion loss of the microstrip line at higher frequencies. Thus, new solutions to improve the roughness of dielectric-copper interface is recommended for high frequency applications.

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