Design and Demonstration of 2.5D Glass Interposers as a Superior Alternative to Silicon Interposers for 28 Gbps Signal Transmission

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***Abstract*—This paper presents the design and demonstration of redistribution layers directly on the surface of glass for high-speed 28 Gbps signaling applications. An unprecedented demand for bandwidth to support cloud and edge computing driven by online services is expected with the continued proliferation of connected devices including smartphones, Internet of Things, and autonomous electric vehicles. High performance systems supporting electrical signal speeds up to and beyond 28 Gbps are required, thus driving the development of advanced multi-chip architectures such as 2.5D interposers. Silicon interposers have been developed and manufactured, but are limited in performance and cost. High conductor and dielectric losses limit maximum data rate, while 300 mm wafer size and expensive damascene processes increase packaging costs. Glass interposers provide similar interconnect densities as silicon but at higher performance and lower cost. The smooth surface roughness (Ra < 10 nm) and low total thickness variation of glass enables fine pitch panel lithography approaching back-end-of-line design rules, while the lower loss tangent of glass and thicker copper metallization reduces dielectric and conductor losses respectively. This work describes the design and demonstration of differential, high-speed traces on a two-metal layer glass interposer. These redistribution layers were fabricated using panel-scalable, semi-additive processes and characterized up to f = 40 GHz using on-panel calibration. Differential crosstalk below 30 dB up to f = 40 GHz was demonstrated without ground shielding at a differential pair spacing greater than 200 µm.**

Keywords – 2.5D interposer; glass interposer; high-speed interconnects; multi-chip modules

I. INTRODUCTION

Demand for online mobile services is driving the need for increased bandwidth not only in consumer electronics, but also in high performance computing to support cloud and edge infrastructure. Furthermore, connected cars have appeared on the horizon as a major new driver of streaming bandwidth. These next generation high performance systems require signal speeds of 28 Gbps and beyond. Silicon interposer packaging architectures have been developed and manufactured to meet these bandwidth requirements. Data rates up to 11.5 Gbps have been demonstrated using a 2.5D silicon interposer fabricated using a four-metal layer back-end-of-line (BEOL) process [1]. The high dielectric losses of silicon, however, limit signal layer assignment. Also, conductor losses are high due to the thin metallization dictated by BEOL processes.

Increased dielectric and conductor losses limit signal length in passive silicon interposers, therefore increasing the driver power required for high-speed signaling. In spite of these challenges, higher data rates have been demonstrated by Xilinx using stacked silicon integration (SSI) and silicon-less interconnect technology (SLIT) [2],[3]. The main difference between these interposer technologies is the effect of through silicon vias (TSV) on performance-critical nets. Signal speeds of 28 Gbps are achieved using SSI where TSV are included in high-speed signal paths. By eliminating TSV and the associated capacitive loading and crosstalk between TSV, SLIT technology can achieve even higher data rates. Both TSV and non-TSV silicon interposer technologies, however, are ultimately limited by high cost. Two contributing factors that increase packaging costs include 300 mm wafer level processing and the need for an additional packaging layer between the interposer and the board to improve second level interconnection reliability and power delivery.

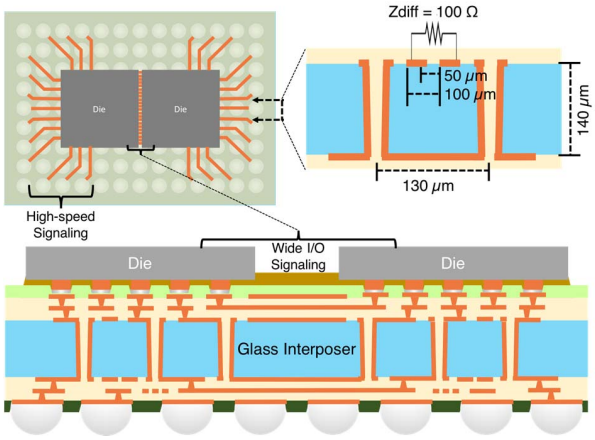

Figure 1. 2.5D glass interposer cross section schematic with top view showing high-speed and wide I/O signal regimes with a detailed cross section of the high-speed interconnect layer.

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Georgia Tech has been developing an alternative interposer technology that addresses the aforementioned challenges of silicon interposer—(1) high electrical loss, (2) high fabrication cost, and (3) additional packaging layers. This paper presents the design and demonstration of a 2.5D glass interposer with differential microstrip transmission lines on bare glass redistribution layers (RDL) for signal speeds up to f = 40 GHz, as shown in Fig. 1. Redistribution layers directly on the glass surface (shown in the detailed cross section of Fig. 1) for high-speed channels leverage the low dielectric constant and low loss tangent of glass to enable higher channel power efficiency compared to silicon interposers. Furthermore, the smooth surface (Ra < 10 nm) and low total thickness variation (TTV) of glass enables RDL line pitch and width similar to back-end-of-line (BEOL) processes across large panels and reduces the conductor-dielectric interface losses. Large glass panel processing up to 510 mm size, compared to 300 mm silicon wafers, results in higher throughput, lower RDL cost, and lower interposer cost. Hence, glass is a compelling low cost and high performance alternative to existing silicon interposer technologies.

This paper is organized into the design, fabrication, and characterization of high-speed RDL on glass. Section II discusses the design of high-speed interconnects on glass interposer based on a two-metal layer stack-up. Section III describes the fabrication of the glass interposer test vehicle using a panel-scalable process flow. Section IV summarizes high frequency characterization of high-speed test structures, and Section V concludes with a discussion of RDL on glass for high-speed interconnects based on current and previous results in [4],[5].

II. Design and Simulation

The design and high frequency simulation of high-speed RDL on glass is described below. The low permittivity and loss tangent of glass along with its availability in large, thin panel formats allows for the implementation of high-speed channels using a differential microstrip line. Ground shielding between high-speed signal lines and the glass substrate is not required. This reduces layer count as well as packaging costs.

A. Test Vehicle Stack-up

A two-metal layer stack-up is assumed for the design of the differential microstrip lines on bare glass where a dry, thin-film photoimageable dielectric (PID) is used as the passivation layer. The high-speed electrical test vehicle stack-up is shown in Fig. 2 along with the dielectric material properties in Table I.

Advantages of this stack-up for high-speed signaling include thick signal and ground layers to reduce conductor losses, as well as build-up layers with negligible loss tangent to reduce losses in the dielectric medium. While the test vehicle presented in this paper is limited to RDL on bare glass, this core stack-up is intended for additional routing layers. These additional routing layers may include fine pitch RDL for die-to-die interconnects typical of 2.5D interposers depicted in Fig. 1, or an optical routing layer as described in [8].

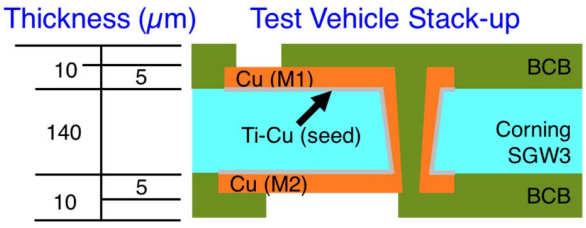


Figure 2. High-speed electrical test vehicle stack-up.

TABLE I. Test Vehicle Material Properties [6],[7]

Material	Permittivity	Loss Tangent
SGW3 Glass	5.30 (15.6 GHz)	0.006 (15.6 GHz)
Dry Film BCB	2.65 (100 MHz)	0.008 (100 MHz)

B. Differential Microstrip Line

Design rules for a differential microstip line were determined from the two-metal layer test vehicle stack-up using a 2D electromagnetic (EM) solver. The design methodology to determine microstrip line pitch and width was similar to the one described in [4], but goes beyond that approach to include the effects of the build-up dielectric layer. First, line widths for a single microstip line were determined that resulted in a single-ended impedance Z_0 = 50 – 100 Ω. Differential microstrip lines were then simulated using line widths from this initial design space as shown in the cutout of Fig. 3. Line pitch, which resulted in a differential line

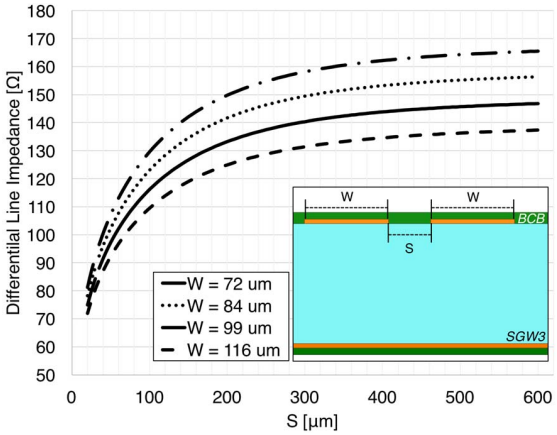


Figure 3. 2D electromagnetic differential line impedance simulation of high-speed RDL on bare glass.

TABLE II. High-Speed Electrical Test Vehicle Design Rules

Design Parameter	Design Specification
Glass thickness	140 μm
Copper thickness	5 μm
Titanium thickness	0.05 μm
Line pitch	150 μm
Line width	100 μm
TPV pitch	150 μm
TPV diameter	75 μm

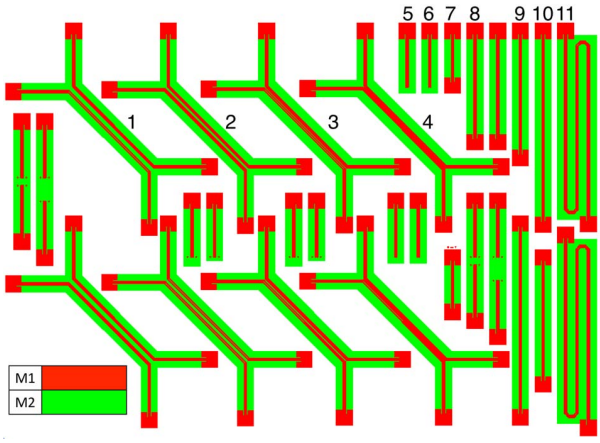


Figure 4. High-speed electrical design test structures on two-metal layer glass interposer test vehicle (TPV at differential signal launch).

TABLE III. HIGH-SPEED ELECTRICAL TEST STRUCTURE SUMMARY

Test Structure	Specification
1	Differential crosstalk (400 µm pair spacing)
2	Differential crosstalk (200 µm pair spacing)
3	Differential crosstalk (100 µm pair spacing)
4	Differential crosstalk (50 µm pair spacing)
5	5 mm short
6	5 mm open
7	5mm thru
8	10 mm thru/line
9	11.4 mm line
10	17.3 mm line
11	48.6 mm line

Test structures 5-11 intended for on-panel calibration

impedance Z_{diff} = 100 Ω, for each corresponding line width was determined using a parametric sweep as shown in the plot of Fig. 3. Final line pitch and width rules were down selected using two criteria:

1. High yield assuming a semi-additive process (SAP).
2. Line pitch matching chip-level bump pitch.

Line pitch was restricted in this case to minimize RDL fan-out, which results in differential line impedance mismatch at the die bump.

The final test vehicle design rules are summarized in Table II based on this design approach and the simulation results. Through-package via (TPV) pitch and diameter were determined based on manufacturer design rules provided by Corning Inc., as well as differential line pitch. Similar to design criterion two above, matching line pitch with TPV pitch reduces losses due to impedance mismatch at this signal transition.

C. Designs for Test

The proposed stack-up is a low cost solution to implement high-speed channels on glass. Due to ground layer proximity, however, differential crosstalk is expected to be higher compared to implementations in build-up layers with thinner dielectric, which affords tighter ground proximity. Differential microstrip line performance on glass has been

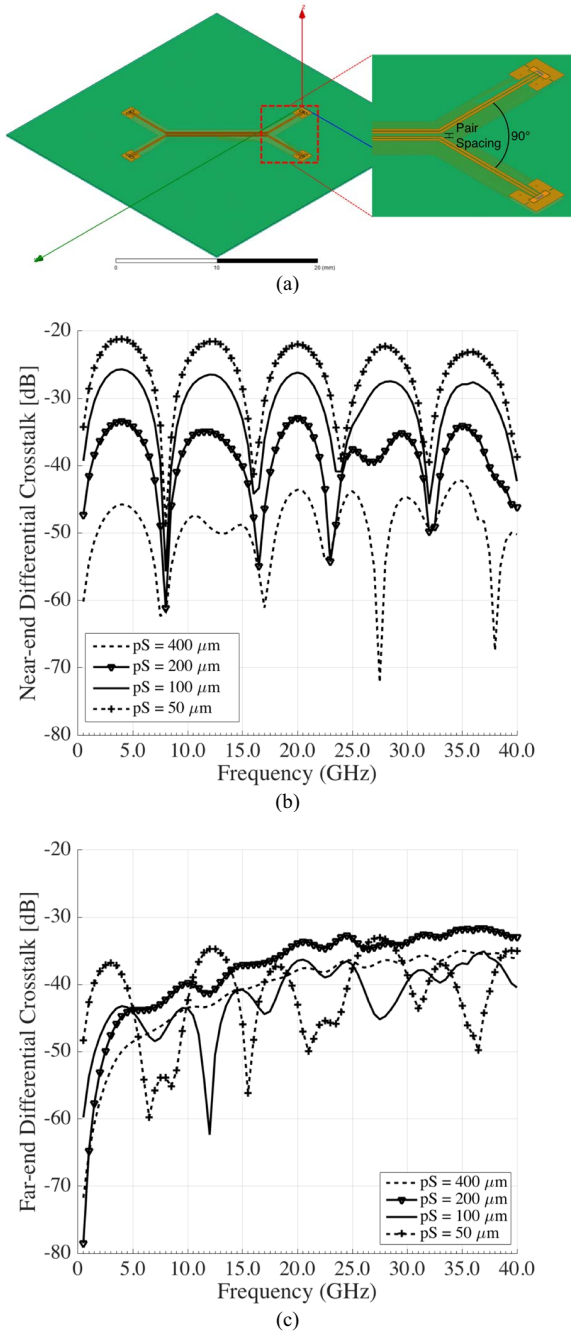


Figure 5. 3D electromagnetic simulation of RDL on glass (a) model for crosstalk, (b) near-end differential crosstalk, and (c) far-end differential crosstalk for pair spacing pS = 50 µm – 400 µm.

shown in [5], where insertion losses as low as 0.05 dB/mm at f = 14 GHz were demonstrated. This low insertion loss is attributed to low conductor and dielectric losses that result from using a stack-up similar to the one shown in Fig. 2. Therefore, the main focus for the electrical test vehicle studied herein is to determine differential crosstalk between these low loss, high-speed channels.

Four crosstalk test structures are included in the test vehicle design with variable differential pair spacing (pS) ranging from pS = 50 µm up to pS = 400 µm as shown in Fig. 4 and Table III. Ground shielding was not introduced in these test structures as the main purpose was to determine a minimum pair spacing design rule to meet crosstalk system requirements at signal frequencies up to f = 40 GHz.

Additional high frequency test structures are included in the design to improve characterization accuracy. These structures include reflection (open and short), thru, and line calibration test structures for vector network analyzer (VNA) measurement. Calibration structures maintain the same stack-up and test vehicle design rules as defined in Table II, as well as a consistent differential signal launch pad design. To support TRL (thru, reflect, line) calibration over a broader frequency range, line structures from L = 10 mm up to L = 48.6 mm are included as a part of this on-panel calibration kit.

D. Crosstalk

Crosstalk between differential microstrip transmission line pairs was simulated using a 3D EM solver. Material properties for the glass panel were modified according to those frequency dependent properties described in [6] to improve simulation accuracy. The model geometry used in the simulation is shown in Fig. 5a in which signal excitation used lumped ports assigned to a ground-signal-signal-ground differential launch pad with dimensions matching those used in test structures shown in Fig. 4. Differential pair spacing was also varied according to the aforementioned crosstalk test structures from 50 µm up to 400 µm.

Near-end and far-end differential crosstalk simulation results at different pair spacing are shown in Fig. 5b and Fig. 5c respectively. As expected, crosstalk improved with increased pair spacing and near-end crosstalk is greater than far-end crosstalk across the frequency range of interest. More importantly, these simulation results indicate that a differential crosstalk less than 30 dB is expected when pair spacing is greater than 200 µm up to f = 40 GHz without ground shielding.

III. FABRICATION

The glass test vehicle was fabricated using a panel-scalable process flow summarized in Fig. 6 on 100 mm x 100 mm x 0.140 ± 0.01 mm via-first glass samples provided by Corning Inc. with a customer procured TPV pattern. A basic clean and plasma (O_2) descum was used prior to metallization on glass. Titanium was used as an adhesion layer at the copper and glass interface by sputtering a titanium-copper (Ti-Cu) seed layer by PVD prior to the SAP. After completing SAP lithography and electrolytic plating, this Ti-Cu seed layer was removed by two sequential etching steps. Copper seed layer removal used a differential spray etching process optimized to minimize copper over etch and maintain line pitch and width; titanium seed layer removal used a hydrofluoric acid flash etching step. Following this SAP to form a two-metal layer RDL on glass, a 10 µm thick benzocyclobutene (BCB) based laminate PID film provided by DOW Chemical was applied using vacuum lamination. For this particular test vehicle, this dry film dielectric serves as passivation layer, but can be used as an interlayer dielectric between a high speed routing layer and additional routing layers. Glass panel fabrication is completed after applying an electroless nickel immersion gold (ENIG) surface finish. High frequency tests, however, were

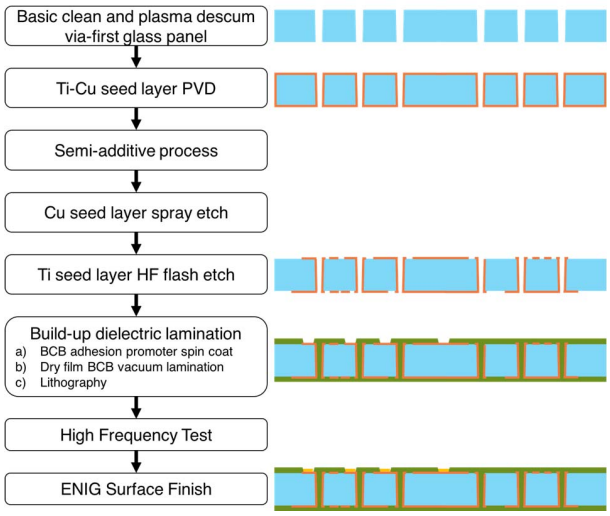
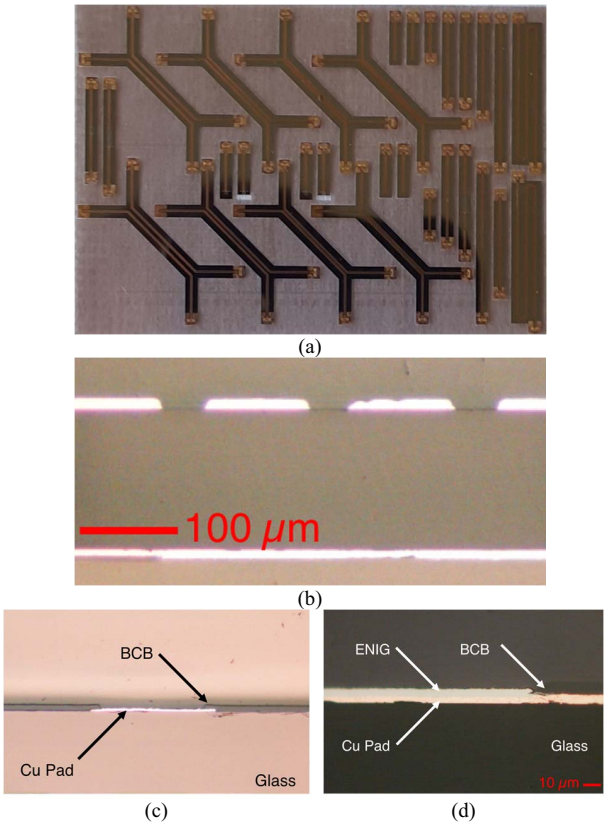


Figure 6. Panel-based process flow to fabricate RDL on bare glass.



(a) (b) (c) (d)

Figure 7. Glass panel fabrication results including: (a) crosstalk test structure overview, (b) differential pair cross section before passivation and cross section details (c) before and (d) after surface finish.

performed prior to this surface finish, therefore they did not consider effects of this metallization.

Glass panel fabrication results are summarized in Fig. 7. Crosstalk test structures for high frequency characterization corresponding to the designs in Fig.4 are shown in Fig. 7a. Before passivation, panel inspection revealed minor pitting in the RDL as shown in the differential pair cross section in Fig. 7b. This fabrication result is attributed to less than optimized electrolytic bath conditions, but panels considered for measurement did not contain significant metallization defects. Fig. 7c shows representative fabrication results after passivation. This cross section confirms sufficient step coverage and adhesion of the BCB-based dry film dielectric to both glass and copper layers prior to high frequency tests. Fig. 7d depicts glass panel fabrication results after surface finish. A standard ENIG process was used to plate an approximately 3 µm thick nickel layer with no indication of delamination of solder mask defined passivation openings.

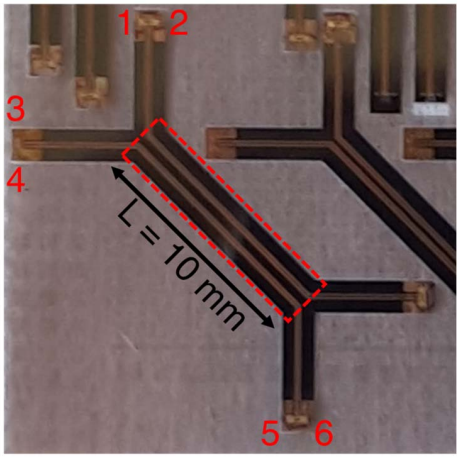
IV. Characterization

Differential crosstalk test structures were characterized using a 6-port VNA measurement calibrated using the aforementioned on-panel calibration structures. The single-ended port assignment for this measurement is shown in Fig. 8a where the remaining ports were terminated with Z = 50 Ω loads. After on-panel calibration, the reference plane was set at the probe tips. Further de-embedding to remove pad effects was not performed due to the test structure geometry. Coupling coefficients between perpendicular differential lines, pads, and probes are negligible since the signal launch pads are orthogonal. Therefore, the resultant differential crosstalk is mainly determined by the area where pair spacing is less than 400 µm and differential pairs are parallel as highlighted in Fig. 8a.

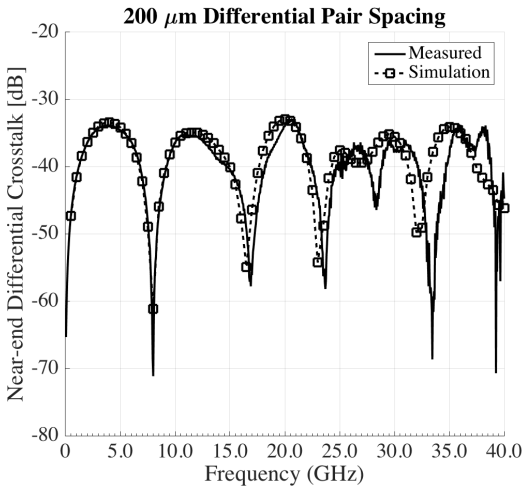
Near-end and far-end differential crosstalk model to hardware correlation at a pair spacing pS = 200 µm is shown in Fig. 8b and Fig. 8c respectively. In both plots, measured results are shown as a solid line and 3D EM simulation results are shown as a dashed line with a square marker. Good correlation is observed up to f = 25 GHz with fair correlation up to f = 40 GHz. A shift in resonance points up to $\Delta f \approx 2$ GHz beyond f = 25 GHz is observed in near-end crosstalk compared to simulations. Deviations between the simulated and measured results are expected for far-end crosstalk measurements due to the low signal strength less than 35 dB. Most importantly, the simulated results predict the maximum differential crosstalk across the measured frequency range and is less than 30 dB for a pair spacing greater than 200 µm without ground shielding.

V. Conclusion

This paper presents the design and demonstration of 2.5D glass interposers with advanced RDL to achieve high signal speed supporting up to 28 Gbps data rates. The low permittivity and loss tangent of glass contributes to this electrical performance for high speed channels with insertion losses as low as 0.05 dB/mm at f = 14 GHz [5]. Furthermore, the smooth surface roughness and low TTV of glass enables line pitch and width similar to that of silicon BEOL but on



(a)



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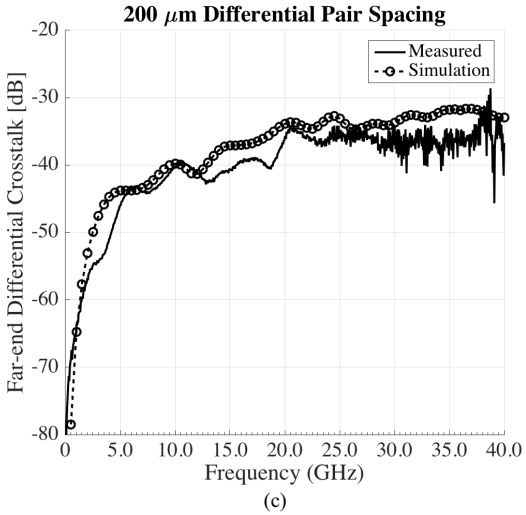

(c)

Figure 8. High frequency measurement (a) port assignment and model to hardware correlation of (b) differential near-end crosstalk and (c) differential far-end crosstalk at 200 µm pair spacing.

large panels using an SAP flow developed in [4] to reduce packaging costs. In this paper, the smooth surface of glass was leveraged to directly fabricate precise transmission lines with critical dimensions close to BEOL ground rules. A panel-scalable process was used to fabricate high-speed channels on 140 μm thin glass to demonstrate differential crosstalk less than 30 dB up to f = 40 GHz. Therefore, using RDL on glass for a high-speed signal layer, as described in this paper does not require ground shielding between high-speed channels and the glass substrate, thus reducing overall package layer count and providing flexible layer assignment to further decrease packaging costs. The integration of high bandwidth photonic interconnects as well as fine pitch chip assembly have also been demonstrated in the glass interposer program at Georgia Tech, leading to a complete high performance system solution.

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