Design, Demonstration and Characterization of Ultra-thin Low-warpage Glass BGA Packages for Smart Mobile Application Processor

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***Abstract*— This paper presents the design, fabrication, assembly, and characterization of a fully-integrated single-chip glass BGA package at 40/80 µm off-chip I/O pitch with multilayered wiring and through-package-vias (TPVs) at 160 µm pitch. The designed test vehicle emulates an application processor package for smart mobile applications, and enables for the first time measurements of DC signal transmission from the die to the board, through the package, at this density and pitch. A daisy chain test die, 10 mm x 10 mm in size, was designed to emulate a logic processor chip comprising 5448 I/Os distributed in four peripheral rows at 40/80 µm pitch and a central area array at 150 µm pitch. The test dies were fabricated and bumped with standard Cu pillars by ASE. The glass package design included four routing layers, with blind vias (BVs) and TPVs both at 150 µm pitch, to connect 176 I/Os to the board, with BGAs at 400µm pitch. Independent multi-level test structures were added for evaluation of TPV and BV yield during fabrication, as well as partial chip- and board-level interconnection yield and reliability. The TPVs in glass were achieved by a via-first process with a high-throughput plasma etching and primer drilling method. Semi-additive processes (SAP), combined with wet chemical surface treatment methods were applied for patterning of the multi-layer wiring with a minimum of 20 µm Cu trace width at 40 µm pitch. A fan-in fan-out finger design was implemented on the top layer for bump-on-trace chip-level interconnections. Chip assembly on glass panels was carried out by high-speed thermocompression bonding with non-conductive paste (TC-NCP) with the new high-performance APAMA chip-to-substrate (C2S) bonder by Kulicke and Soffa. Yield of each process step was evaluated through fabrication and assembly by DC electrical characterization of TPV, BV and chip-level interconnection daisy chains. Die-to-substrate interconnections were characterized, demonstrating signal transmission through the fully-integrated glass package for the first time at this I/O pitch.**

Keywords – ultra-thin glass BGA package; mobile; via-first; high speed TCB.

I. INTRODUCTION

Increasing demands for mobility, functionality and performance in smart mobile systems have been driving off-chip interconnection pitches to below 40 µm. Pitch scaling is also accompanied by an increase in die and package sizes, raising concerns for chip-level reliability [1, 3].

Low-CTE substrates, such as silicon interposers and low-CTE organic packages, were introduced to address this challenge. These substrates, however, exhibit a large CTE mismatch to the board, therefore shifting reliability concerns to board level. These concerns are further aggravated with the trending reduction in substrate thickness to meet the needs for improved power delivery performance [3], and system miniaturization, bringing increased solder strains and warpage [2, 5]. Ultra-thin organic substrates, with their relatively low elastic modulus (~20-35 GPa) and glass transition temperatures are especially at risk, hindering their scalability to package sizes above 20 mm × 20 mm [4]. Beyond conventional organic packages, silicon interposers have been proposed as an alternative solution, in particular for high-performance packaging with high-density interconnections. However, the wide-scale adoption of silicon interposers is limited by the poor electrical performance due to the high permittivity and high loss tangent of silicon, as well as their prohibitive fabrication cost.

Glass packaging has recently emerged as a promising system integration technology that addresses all aforementioned challenges. Glass, owing to its exceptional dimensional stability, enables silicon-like lithographic resolution, at low-cost given by double-side panel-scale processing [5]. Glass also benefits from outstanding dielectric properties and potential enhancements in signal distribution network (SDN) / power distribution network (PDN) performance with thickness reduction below 100 µm [6]. The improved PDN performance and reduced core thickness enable smart mobile devices to have lower power

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consumption and smaller package form factors. Furthermore, due to its high modulus, glass exhibits significantly lower die warpage than organics with same CTE [7]. Therefore, glass has compelling benefits over organic packages in I/O pitch and warpage mitigation, and over silicon interposers in electrical performance and cost, making it an ideal platform for packaging of consumer products, in particular mobile logic devices [8].

This paper reports the design and demonstration of a fully-integrated, single-chip, glass BGA package, emulating an application processor package for mobile applications with a "logic" daisy-chain die at 40/80 µm pitch, as shown in Fig. 1.

The designed package integrates several basic technologies, such as TPVs, multi-layered wiring, chip assembly by thermocompression bonding and SMT process at 15mm package size, all individually testable, to provide the first process monitor to help analyze the system-level yield and reliability of glass packaging. The main contributions of this work include: 1) first-time demonstration of DC signal transmission from the die through a four-metal layer 100µm-thick glass package with TPVs to the board and back at 40/80 µm off-chip I/O pitch; 2) advanced via-first through package via (TPV) processes with high-throughput plasma etching method to open the primer; and 3) high-speed thermocompression bonding at panel level. Design, fabrication, assembly and characterization of the test vehicle are detailed in the following sections.

II. DESIGN

To demonstrate this glass packaging technology, dummy test dies with daisy chain structures were fabricated by ASE Group on 300 mm wafers, as shown in Fig. 2 (a), to emulate logic dies. The die is designed at a standard size of 10 mm x 10 mm to emulate high-end Application Processors (AP), with 1856 signal I/Os at 40/80 µm pitch in 4 peripheral staggered rows and 3592 power I/Os at 150 µm pitch in a central area array, for a total of 5448 I/Os as shown in Fig. 2 (b) and (c).

A four metal layer fully-integrated glass package was designed to connect all 5448 chip I/O bumps to the substrate. Among the chip I/O bumps, 176 of those were connected through chip-level interconnections, and TPVs, and board-level interconnections to the board. The top view of the glass package layout design is shown in Fig. 3 (a), which includes the layout of four metal layers, top and bottom solder resist, as well as the location of BVs and TPVs. This fully-integrated glass substrate design coupon, which measured 15 mm x 15 mm, was then panelized to fit in a 150 mm x 150 mm glass panel. Due to the exposure range of the projection aligner used (provided by Ushio Inc.), which is a 100 mm circle, the coupon is laid out in a 5 x 3 array with 0.5 mm dicing street, and exposed twice to achieve 30 coupons in a panel, as shown in Fig. 3 (b).

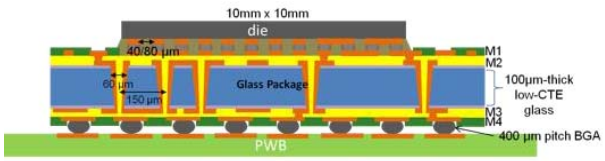


Figure 1. Cross section of a fully-integrated glass BGA package with 40/80µm minimum I/O pitch.

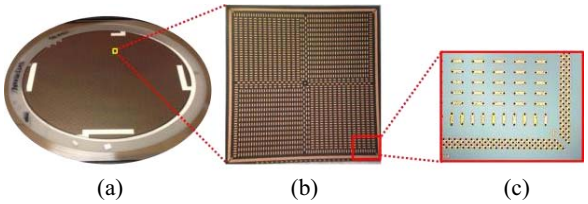


Figure 2. Daisy chain test dies fabricated by ASE (a) on 300 mm wafer, (b) one single die from the 300 mm wafer, and (c) snap shot of die corner.

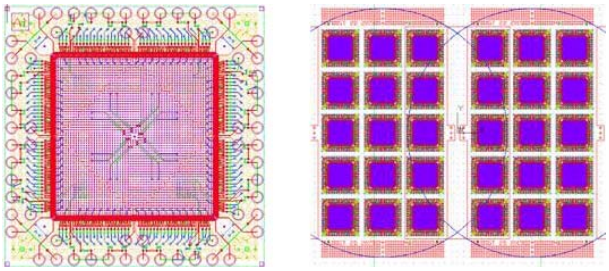


Figure 3. Top view of substrate layout design of (a) single fully-integrated glass package coupon at the size of 15mm x 15mm x 0.1 mm, and (b) 30 coupons in total on a 150mm x 150mm glass panel.

Multi-level test structures were designed to evaluate the yield at each fabrication process step, as shown in Table I. Nine types of test structures were designed, including TPV daisy chains, BV daisy chains, chip-level interconnection daisy chains, and other multi-layer test structures. The first five types are substrate-level test structures to be tested during each phase of substrate fabrication for yield evaluation. The last five types require the assembly of the dummy die. Only type 7 require board level assembly, as the primary focus of present study is on the reliability of die-to-substrate interconnections. Type 8 and type 9 are the most extensive test structures, with the only difference being the inclusion of bottom blind via & M4 for type 9 test structures.

Relatively relaxed design rules based on previously achieved results were applied to optimize the yield to focus the study of process variability in fabrication and assembly. The design rules are summarized in Table II. The minimum line and space is set at 20/20 µm to facilitate yield, but has limited routing capability in the 40/80 µm pitch signal I/O area. As a result, fine line escape routing is not included in the test structures.

TABLE I. MULTI-LEVEL TEST STRUCTURES FOR YIELD EVALUATION

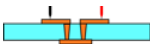
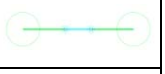
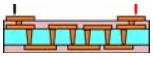
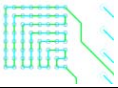
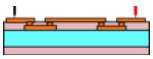
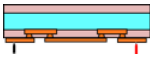
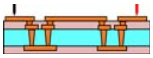
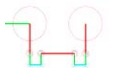
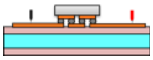
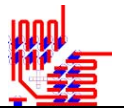
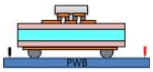
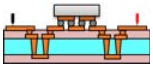
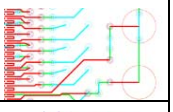
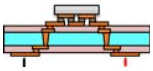
Type	Schematic	Layers	Description	Top View Layout
1		M2-M3	TPV chains	
2		M1-M3		
3		M1-M2	BVs	
4		M3-M4		
5		M1-M3	Substrate	
6		Die-M1	Chip-level DCs	
7		M4-PWB	Board-level DCs	
8		Die-M3	CLI + Substrate	
9		Die-M4	CLI + Substrate	

TABLE II. SUMMARY OF DESIGN RULES

Design Rules			
Glass thickness	100 µm	Min. L/S	20/20 µm
Glass body size	15 mm x 15 mm	BV diameter	80 µm
Logic die size	10 mm x 10 mm	BV pitch	Min. 150 µm
Chip-level pitch	40/80 µm	TPV diameter	60 µm
BGA pitch	400 µm	TPV pitch	Min. 150 µm

III. FABRICATION

The fully-integrated glass packages were fabricated on a 150 mm x 150 mm low-CTE glass panel that is 100 µm thick. The illustrated fabrication process flow and stack-up specifications of the fully-integrated glass package are shown in Fig. 4 and Table III respectively.

In this test vehicle, TPVs at 150 µm pitch were achieved by a via-first process, which utilized via formation on bare glass by Asahi Glass Company, followed by primer lamination and opening with a high-throughput plasma etching method. The primer material used is a dry-film dielectric provided by Ajinomoto Inc., called ABF, which can be processed at a low temperature of 180°C. In addition, the surface of ABF is suitable for electro-less plating of copper seed layer, which allowed the use of semi-additive process (SAP). SAP utilizes electrolytic plating of lithographically defined patterns on the copper seed layer to pattern multi-layer copper traces at a minimum of 20/20 µm line and space. Finer pitch could be achieved by optimization of copper seed layer etching, but was not pursued in this design to maximize yield. To create four metal layers, two SAP steps were performed. The first SAP step was responsible for patterning M2 and M3, as well as the conformal plating of TPVs. ABF was used again as the dielectric layer between the first-level metallization and second-level metallization. The blind microvias were formed by laser drilling of ABF and electro-less plating of both the ABF surface and the via sidewalls. The second SAP step completed the patterning of M1 and M4, as well as the conformal plating of blind vias on either sides of the glass panel.

The passivation layer used is a dry-film based material provided by Hitachi Chemical. Similar to ABF, this material can be processed at a low temperature of 180°C. The pad connections to the die cannot be solder mask defined as the pitch requirement exceeded the capability of the dry-film material. Instead, a bump-on-trace routing structure was

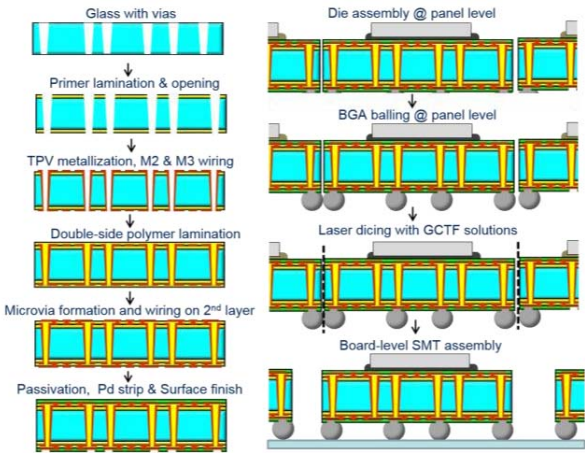


Figure 4. Fully-integrated glass package fabrication process flow.

TABLE III. FULLY-INTEGRATED GLASS PACKAGE STACK-UP SPECIFICATION

	Thickness (µm)	Material	Resource
Solder Resist	10~15	SR-FA	Hitachi Chemical
1st layer polymer	5	ABF GX-92P	Ajinomoto
2nd layer polymer	15	ABF GX-92	Ajinomoto
Glass	100	EN-A1	Asahi Glass Company

used as shown in Fig. 5. Two main fabrication challenges from previous fabrication cycles can be improved by applying such fan-in fan-out bump-on-trace routing structure. One is the surface finish bridging caused by extraneous plating of nickel on the Cu trace with small features, and the other one is the difficulty to have small, individual passivation openings to support the fine-pitch signal I/Os. The bump-on-trace routing structure brings coarser Cu trace width and spacing design rules, and thus reduces the surface finish bridging risk. Further, it accommodates a slit solder resist opening, providing better passivation alignment accuracy and avoiding the passivation resolution challenge.

The bump-on-trace structure does have one additional process requirement: the use of pre-applied underfill materials for chip-level assembly to confine the solder and limit its spread over the exposed trace due to slit opening.

Based on the process flow described above, twelve glass panels and six organic panels as dummy samples were fabricated in three batches. Fig. 6 (a) shows the fabricated glass substrate on a 150 mm x 150 mm square glass panel, while Fig. 6 (b) shows the cross-section of the glass substrate with Cu traces on four metal layer, TPVs of ~60 µm diameter (Fig. 6 (c)), and BVs of ~90 µm diameter (Fig. 6 (d)), which enables the signal to travel from M1 to M3 through BVs and TPVs, and back to M1.

As shown in Fig. 4, once surface finish, usually by a wet process such as electroless nickel immersion gold (ENIG) plating, is applied, substrate processing is considered completed.

Yield for each fabrication process was evaluated by DC resistance characterization of the multi-level test structures listed in Table I.

TPV yield was evaluated on a 75 mm x 150 mm glass half-panel, which consists of 15 coupons in total, as shown in Fig. 7 (a). For each coupon, DC resistances of TPV daisy-chain test structures which connect 264 TPVs in total were measured to calculate the TPV yield of each coupon. As shown in Fig. 7 (b), an over 99% TPV yield, was achieved by via-first process with plasma etching primer drilling method.

Based on the TPV yield evaluation result, the failure metallized via was found and observed, which is shown in Fig. 8. It is observed that the Cu failed to plate around the through package via.

Similarly, the BV yield of 12 coupons was evaluated based on the measurement of DC resistances of BV daisy-chain test structures, as shown in Table IV.

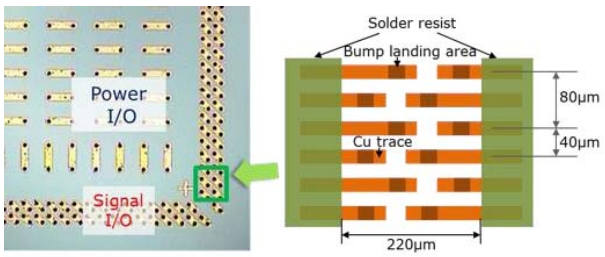


Figure 5. Bump-on-trace structure for die signal I/Os.

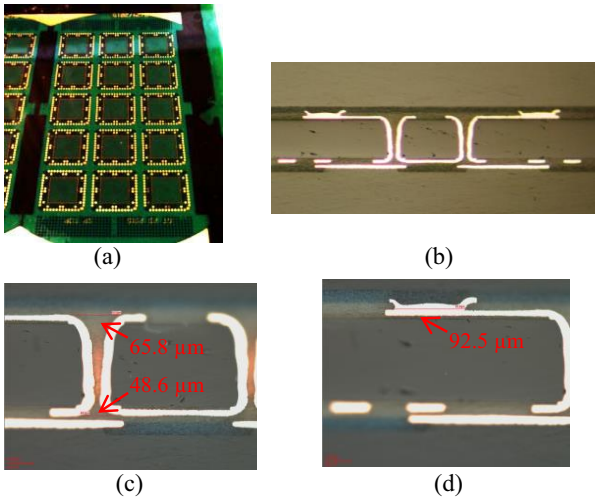
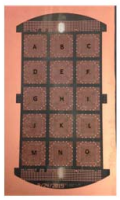


Figure 6. (a) Fabricated glass substrates on a 150mm x 150 mm square glass panel. (b) Cross-section of the glass substrate at 20x magnification, (c) TPV at 50x magnification, (d) BV at 50x magnification.



(a)

Test Structure	Yield Evaluation		
	100%	100%	100%
	100%	99%	100%
	100%	100%	100%
	99%	100%	100%
	100%	99%	100%

(b)

Figure 7. TPV yield evaluation on (a) a 75mm x 150 mm square glass panel. (b) Test structure and TPV yield results.

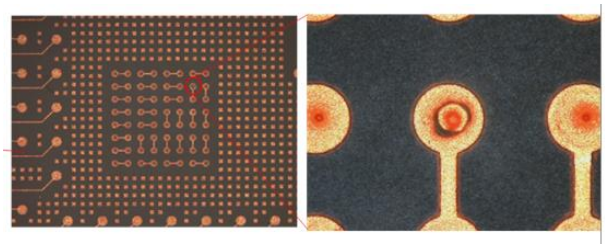


Figure 8. TPV failure observation.

TABLE IV. BV YIELD EVALUATION RESULTS

Test Structure	Yield Evaluation		
	75%	75%	75%
	75%	100%	100%
	100%	50%	75%
	75%	75%	75%
	100%	100%	100%
	100%	50%	50%
	100%	75%	100%
	100%	100%	100%

Excellent yield was therefore confirmed for each substrate-level process step. The die assembly, performed at panel level, is described in the next section.

IV. Chip-level Assembly

Die-to-glass panel assembly was achieved by thermo-compression (TC) bonding with the novel, high-speed, chip-to-substrate (C2S) APAMA fully-automated production bonder from Kulicke and Soffa. The glass substrates, diced into 75 mm × 150 mm halves, were first cleaned with isopropanol alcohol, dried with a N_2 gun, then baked for one hour at 150°C. Non-conductive paste (NCP) from Namics Corporation with a filler content of 50-65% was then precisely dispensed on each bonding sites to an equivalent volume of 18 mg, in a star pattern. The temperature of the stage onto which the substrates were vacuum-held was maintained at 70°C throughout the process. Such low stage temperatures are required, given the typical thermal stability on stage of epoxy-based NCPs, to guarantee no evolution in the material's properties for at least the time it takes to fully populate a substrate strip. The tool head temperature, on the die side, was first ramped up to 120°C with an 800 ms dwell time and a maximum ramp rate of 200 K/s, then to the peak temperature of 300°C, maintained for 2 s. A bonding force of 40 N was applied through the whole process. An assembled glass substrate strip, comprising 15 dies bonded with the described TC process, is shown in Fig. 9.

The underfill fillet size was found uniform and well controlled across a strip. Further, absence of voiding in the NCP layer was confirmed by scanning acoustic microscopy (C-SAM), as seen in Fig. 10.

The cross-section of an assembled coupon in Fig. 11 shows well-formed bump-on-trace Cu pillar inter-connections, with the typical shape expected from TC-NCP processing. Good alignment and solder collapse were achieved with optimized bonding conditions. No significant filler entrapment could be observed within the solder.

Additionally, the assembled strips were found very flat after chip-level assembly, on account of the high modulus (~80 GPa) and glass transition temperature (~550°C) of glass which enabled lower warpage compared to organic substrates of same CTE [7]. Warpage mitigation constitutes one of the key benefits of glass packaging, suggesting potentiality of extending direct SMT assembly of glass BGA packages to the board at body sizes larger than achievable with current packaging technologies, with improved board- and system-level reliability.

Assembly yield was assessed by DC measurements of the chip-to-M1 daisy-chain resistances, including four corner and four inner chains with 20 and 58 bumps, respectively. The results of this evaluation are reported in Table V for three fully-integrated coupons with full yield at package level. All but one chain were electrically functional, with little discrepancies in resistance values between coupons, suggesting a high chip-level assembly yield. The cause of failure is presently undetermined.

After confirming the yield of all individual fabrication and assembly process steps, die-to-substrate interconnections were further characterized by measurement of the signal transmission daisy chains, from die to BGA, as described in the next section.

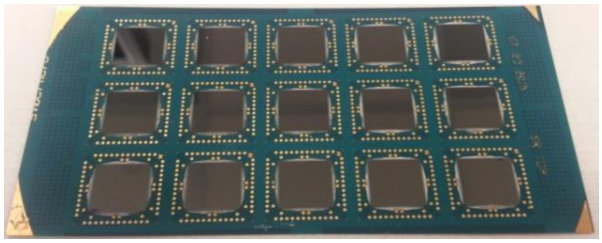


Figure 9. Glass substrate strip after die assembly by TC-NCP.

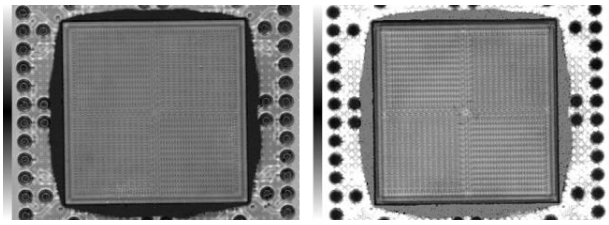


Figure 10. C-SAM images of die-to-NCP interface (left) and NCP-to-glass substrate interface (right).

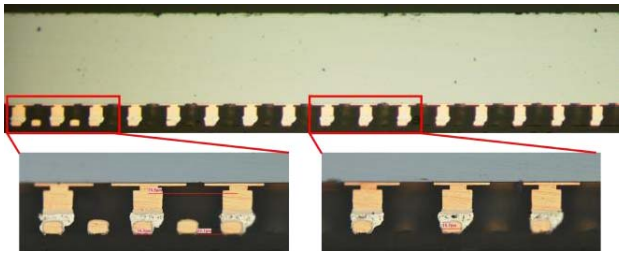


Figure 11. Cross-section of a singulated glass package.

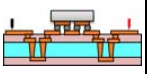
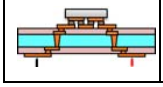
TABLE V. Chip-level Assembly Yield Evaluation

Coupon	Corner Chain Resistance (Ω)				Inner ChainResistance (Ω)			
1	1.23	1.43	1.34	1.23	2.78	3.13	×	2.85
2	1.20	1.54	1.80	1.36	3.17	3.42	3.69	3.27
3	1.45	1.45	1.40	1.51	3.40	3.35	3.61	3.56

V. Characterization of Signal Transmission Through Fully-integrated Glass Package

The DC resistance value of type 8 and 9 multi-level, die-to-substrate test structures, measured on a single coupon, are reported in Table V. The four columns of DC resistance were measured at four different locations of the test structures, uniformly distributed across the coupon. For the same type of structure, the variation of resistances measured at different locations is possibly caused by process variability, such as copper thickness non-uniformity over the glass panel during electrolytic plating. The DC signal transmission from the die through a four-metal layer 100µm-thick glass package with TPVs at this density and

TABLE VI. DIE-TO-PACKAGE INTERCONNECTION YIELD

Test Structure	Layers	Description	DC Resistance (Ω)			
	Die-M3	Signal from Die to M3	1.22	1.03	×	1.08
	Die-M4	Signal from Die to M4	1.21	×	1.67	2.72

pitch was, for the first time, demonstrated by the successive measurements of the test structures shown in Table VI.

VI. CONCLUSIONS

This paper presented the first demonstration of DC signal transmission from the die at 40/80 µm I/O pitch, through a 100 µm-thick glass package with TPVs and multilayered wiring, to the board and back. The designed test vehicles emulated in pitch and size an application processor package for smart mobile applications. The design integrated multi-level test structures for yield evaluation of individual fabrication and assembly process steps, and study of variability in glass package processing at 150 mm x 150 mm panel scale. High TPV yield was achieved at 160 µm pitch, for the first time, by advanced via-first processes with plasma etching primer opening method. Excellent control of BV formation and substrate copper metallization processes was also confirmed by the excellent yield of multi-level TPV and BV daisy chains, with little variation in resistance values. Chip-level assembly was subsequently achieved by standard Cu pillar TC-NCP process on substrate strips, using for the first time a production bonder with high heating rates up to 200 K/s. Chip-to-substrate interconnections were eventually characterized with DC signal transmission demonstrated by probing of die-level I/Os on the BGA side. Such package integrating a number of basic technologies in ultra-thin glass – via-first TPVs, double-side multilayered wiring, Cu pillar die assembly, and SMT at 400 µm pitch – all testable independently and as a whole is an ideal test vehicle to later study reliability and identify critical failure modes and mechanisms to fully demonstrate the glass packaging technology.

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