Electrical Comparison between TSV in Silicon and TPV in Glass for Interposer and Package Applications

Jialing Tong, Kadppan Panayappan, Venky Sundaram, and Rao Tummala, *Fellow, IEEE*
3D Systems Packaging Research Center
Georgia Institute of Technology
Atlanta, GA USA
e-mail: jtong@gatech.edu

***Abstract*—This paper presents one of the first comprehensive studies comparing the electrical performance of through-silicon-vias (TSVs) in silicon with through-package-vias (TPVs) in glass, considering electromagnetic field distributions, 50 ohm impedance design, and the effect of via taper. First, the electric and magnetic field distributions were analyzed using a 3D EM solver (CST Microwave Studio) for the scenario of a signal via adjacent to a return via, to study the differences in the field distributions for TSVs and TPVs. Next, the design for 50 Ω impedance matching was studied with various ground-via configurations for TSVs in silicon and TPVs in glass. It was found that additional ground vias improved the impedance matching to 50 Ω in the high frequency above 40 GHz. Finally, the effect of the via taper on the impedance and insertion loss of TSVs and TPVs was studied, concluding that taper has a positive impact in the case of TSVs in lossy silicon at low frequencies as it reduces the parasitic capacitance while taper has a negative impact in the case of TSVs in intrinsic silicon and TPVs in glass, as it increases the parasitic inductance.**

Keywords: through-silicon-via; through-package-via; silicon; glass; field; impedance; taper

I. INTRODUCTION

Three-dimensional (3D) interconnections with through-silicon-vias (TSVs) have been and continue to be developed to enable increased bandwidth, reduced latency, and lower power consumption [1]. Although 3D IC stacking has seen limited use in memory and image sensors due to thermal and cost challenges, TSV based silicon interposers were used by Xilinx to demonstrate 28 Gbps field-programmable gate array (FPGA) systems using a 2.5D architecture [2]. The main challenges facing silicon interposers are the high cost due to the small wafer size and complex fabrication processes, as well as the significant electrical loss associated with silicon. To address these limitations, Georgia Tech has proposed and demonstrated glass interposer as a lower cost and higher performance alternative to silicon interposers, enabled by the ultra-low loss, silicon-matched coefficient of thermal expansion (CTE), smooth surface, large panel processability, and excellent dimensional stability of glass [3, 4]. Glass is electrically different from silicon, as glass is essentially an insulating material while silicon is a semiconducting material. The term through-package-vias (TPVs), was coined by Georgia Tech to represent lower cost and higher performance vertical interconnections in glass packages and interposers.

There has been a significant amount of research done in the past to understand the fundamental electrical behavior of TSVs in silicon. Due to the SiO_2 liners used in TSVs, a parallel-plate waveguide realized in this structure was first theoretically analyzed and experimentally verified, concluding the existence of three fundamental modes inside, namely slow-wave mode, dielectric quasi-TEM mode and skin-effect mode depending on the resistivity of the silicon substrate and the operation frequency [5]. Then, a high-frequency circuit model was proposed for wafer-lever, chip-level and interposer TSVs, considering these three modes, and closed-form expressions were provided for calculating the transmission-line parameters of TSVs to capture the frequency-dependent modes [6]. Later, comparative modeling was presented for single-ended ground-signal (GS) and ground-signal-ground (GSG) TSVs, which was validated by the measurement results from a double-sided probing system [7]. Based on the TSV modeling research, several design guidelines were presented from 3D EM simulations, namely: a) that little degradation in rise time happens when a signal propagates along the TSVs; b) that the TSV radius should be optimized for better $S_{21;}$ and c) that the tapered-shape TSVs were preferred in terms of electrical performance [8]. Alternate TSV structures, such as coaxial TSVs, were also analyzed, concluding that coaxial TSVs were superior to other TSVs because of their smaller time constants and frequency-dependent dynamic power [9].

There has been limited published research on TPVs in glass, and recent literature on high frequency modeling and characterization of glass TPVs is summarized here. A precise *RLGC* circuit model was proposed and verified for single-ended GS TPVs in glass, with expressions for *RLGC* as a function of design parameters [10]. A TPV array, consisting of one signal TPV and six grounded TPVs, was analyzed through simulation and measurement at 0.1 GHz - 20 GHz, and it was found that such a TPV array had identical characteristics to a coaxial TPV [11]. The insertion loss of metallized TPVs was measured till

40 GHz for wafer-level RF MEMS packaging [12]. The resistance and inductance of TPVs formed by a focused electrical-discharge method were characterized up to 30 GHz, demonstrating negligible loss from TPV transitions and the ultra-low inductance of TPVs [13].

This paper reports on one of the first comprehensive studies comparing the electrical behavior of TSVs in silicon and TPVs in glass in terms of the electromagnetic field distribution, design for 50 Ω impedance, and the effect of via taper. Due to the different electrical conductivities, the fields around TSVs in silicon differ from those around TPVs in glass, resulting in different insertion losses, and this will be analyzed through 3D electromagnetic (EM) simulation in Section II. The impedance for different via configurations will be presented in Section III, leading to design guidelines to achieve 50 Ω impedance matching by introducing multiple ground vias. Finally, the effect of via taper will be investigated in Section IV using 3D EM solvers.

II. Electromagnetic Field Distribution

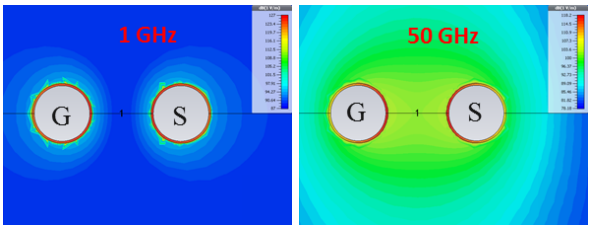
The electromagnetic field distribution around vias is important, as the electric field and the magnetic field are directly related to the via capacitance and inductance, respectively. Detailed analysis of the EM field distribution around TSVs in silicon and TPVs in glass was performed using a 3D EM solver (CST Microwave Studio) [14]. The material properties used in the simulations are listed below in Table I.

A. EM Field

The GS configuration of a 30 µm (diameter) signal TSV adjacent to a 30 µm (diameter) ground TSV at minimum 60 µm pitch in lossy silicon was simulated in CST and the electric field strength is plotted in Fig. 1. The silicon dioxide layer has a thickness of 1 µm for each TSV. It can be seen from Fig. 1 (a) that at 1 GHz, almost all the electric field is confined in the silicon dioxide, which is characteristic of the slow-wave mode. The reason for this is because the conductivity of the lossy silicon, quantitatively 10 S/m, is much larger than $\omega\varepsilon$=0.66 S/m at 1 GHz, which implies that the EM wave at 1 GHz sees 10 S/m silicon as a good conductor and the electric field cannot penetrate through it. Due to the confined electric field, there is a strong capacitance in the silicon dioxide layer. On the other hand, when the operation frequency increases to 50 GHz and $\omega\varepsilon$ increases to 2.78 S/m that is comparable to the silicon conductivity, the EM wave at 50 GHz sees the silicon as a high-loss dielectric and the electric field starts to penetrate through silicon, as shown in Fig. 1 (b). This is the characteristic of the dielectric quasi-TEM mode.

TABLE I Material Properties

Characteristic	Silicon	Glass
Dielectric Constant	11.7	5-7
Loss Tangent @ GHz	1.511@10 (lossy) 0.015@10 (intrinsic)	0.005
CTE (ppm/K)	3	3-8.5
Surface roughness (nm)	0.15-0.3	<1
Water absorption	0	0
Young's Modulus (Gpa)	130-185	50-90



(a) (b)

Figure 1. Electric field strength for GS TSVs in lossy silicon at (a) 1 GHz and (b) 50 GHz.

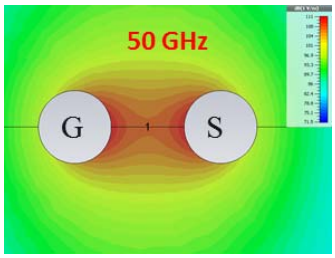


Figure 2. Electric field strength for GS TPVs in glass at 50 GHz.

Unlike TSVs in lossy silicon where the fields change with the frequency, TSVs in intrinsic silicon (σ=4.27×10^{-4} S/m) have almost identical field distribution to Fig. 1 (b) across all frequencies, because $\omega\varepsilon$ is always much larger than the silicon conductivity and the EM wave sees the intrinsic silicon as a low-loss material.

Similarly, such GS via was simulated for the case of glass, with the top view of the electric field strength plotted in Fig. 2. Thanks to the high resistivity of the glass, the EM wave at any frequency also sees glass as a low-loss material, and the field starts from one TPV and terminates at the other one.

B. Insertion Loss

The simulated insertion loss per unit length is shown in Fig. 3 for the aforementioned GS vias in lossy silicon, intrinsic silicon and glass. Overall, the insertion loss per unit length of GS TSVs in lossy silicon is the highest, while that of GS TSV in intrinsic silicon is higher that of GS TPV in glass. Thus, it can be concluded that TPVs in glass have better electrical performance over TSVs in silicon. Another key difference between these three cases is that the insertion loss per unit length for TSVs in lossy

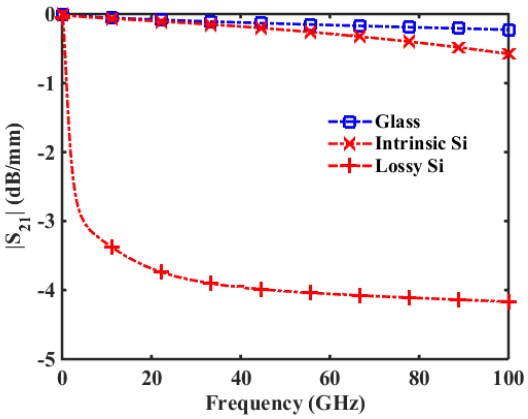


Figure 3. Insertion loss per unit length as a function of frequency for GS vias in lossy silicon, intrinsic silicon and glass.

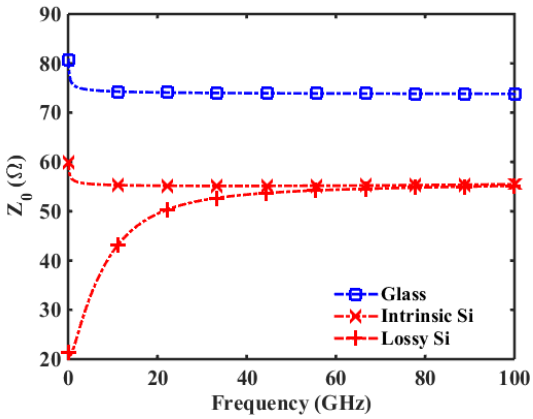


Figure 4. Impedance as a function of frequency for GS vias in lossy silicon, intrinsic silicon and glass.

silicon decreases drastically below 20 GHz, and eventually exhibits a linearly decreasing behavior. The reason for the steep rate at low frequency is that the slow-wave mode excited at these frequencies is a lossy wave mode with higher attenuation constant.

III. 50 Ohm Impedance Matched Designs

In most cases, vias are electrically short, because the wavelength of the highest frequency of interest is still ten times longer than the geometric length of vias. This implies that it is reasonable to approximate vias as lumped elements within the acceptable range of numerical accuracy. But, as the data rate and the operation frequency continue to increase, the accuracy is improved by treating vias as transmission lines. Given a specific substrate thickness, Table II summarizes the critical frequency above which vias have to be treated as transmission lines for better accuracy.

A. Impedance

The impedance of GS vias was simulated for the case of lossy silicon, intrinsic silicon and glass. According to the results depicted in Fig. 4, the impedance of GS TSVs in lossy silicon increase from 20 Ω at low frequency, rises quickly up to 52 Ω at 30 GHz, and settles at 55 Ω which is identical to the impedance of GS TSVs in intrinsic silicon. This frequency-dependent impedance confirms the EM mode transition as described in the previous Section II. In contrast, the impedance of GS TPVs in glass settles around 74 Ω, and that of GS TSVs in intrinsic silicon settles around 55 Ω. This impedance difference between them mainly arises from the different dielectric constants as shown in Table I.

TABLE II Critical Frequency

SUB THK (μm)	λ/10 (mm)	$f_{c,\,Si}$ (GHz)	$f_{c,\,glass}$ (GHz)
300	3	28.99	44.50
100	1	86.97	133.50
50	0.5	173.93	267.00

Using the transmission line parameters for two wires [15], the impedance of GS vias in intrinsic silicon and glass can be calculated by the following equation as

$$Z_0 = \frac{\cosh^{-1}(p/D)}{\pi} \cdot \sqrt{\frac{\mu_0 \mu_r}{\varepsilon_0 \varepsilon_r}} \qquad (1)$$

where Z_0 is the impedance of GS vias, p is the center-to-center pitch between the signal via and the ground via, D is the diameter of the vias, μ_0 and ε_0 are the vacuum permeability and vacuum permittivity, respectively, and μ_0 and ε_0 are the relative permeability and relative permittivity of the substrate, respectively. Since the GS vias in lossy silicon were reported earlier [6], their frequency-dependent impedance is not considered in this paper.

To validate the impedance computed by equation (1) against that calculated by 3D EM solver, the pitch-to-diameter ratios were varied from 2 to 10 for 18 μm, 30 μm and 60 μm diameter vias in intrinsic silicon and glass. The results are presented in Fig. 5, and the maximum relative error between the computation and simulation is less than 8% for the case of intrinsic silicon and less than 2% for the case of glass. Equation (1) was found to be more accurate in estimating the impedance values for TPVs in glass due to the fact that the silicon dioxide liner in TSVs is ignored while deriving (1).

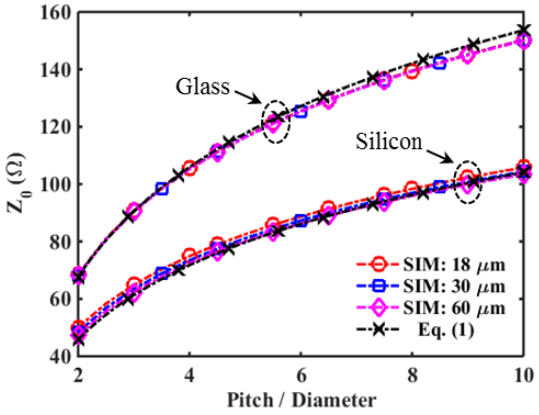


Figure 5. Impedance as a function of pitch-to-diameter ratio for GS vias in intrinsic silicon and glass.

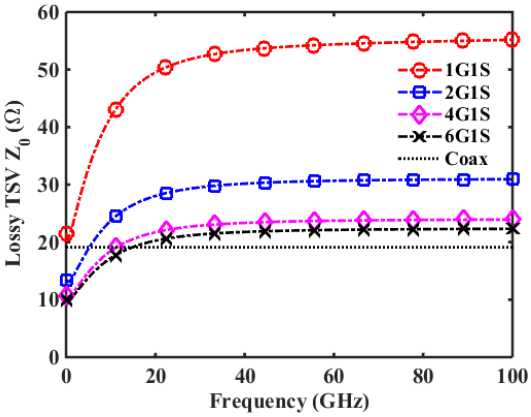


Figure 7. Impedance as a function of frequency for various TSV configurations in lossy silicon.

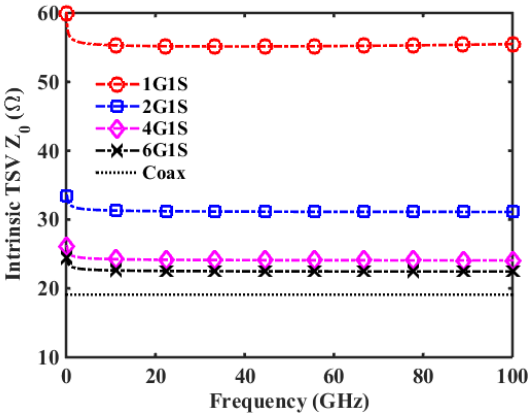


Figure 8. Impedance as a function of frequency for various TSV configurations in intrinsic silicon.

B. Ground Via Configuration

As discussed in Section III-A, the impedance of GS vias in either silicon or glass at high frequency is higher than the widely used 50 Ω. Better impedance matching can be achieved by introducing additional ground vias around a signal via. By doing so, the capacitance between the signal and the ground will be increased, resulting in a lower impedance value.

The four via configurations shown in Fig. 6 were studied, including the GS via configuration. Fig. 6 (a) illustrates two ground vias adjacent to one signal via (2G1S or GSG); Fig. 6 (b) illustrates four ground vias with one signal via (4G1S); Fig. 6 (c) illustrates six ground vias with one signal via (6G1S); Fig. 6 (d) illustrates the coaxial via [9]. The ground vias were placed at the minimum pitch to the signal via, for all scenarios. All five via configurations were first simulated and then compared for the case of lossy silicon. The simulation results given in Fig. 7 show that the impedance trend with frequency for each via configuration is similar, except for the coaxial via. As there is a strong capacitance associated with the SiO_2 liner at low frequencies, and the impedance is already lower than 50 Ω, adding ground vias makes the impedance even lower, exacerbating the impedance mismatch to 50 Ω. So, at low frequencies where the EM mode is slow-wave mode, inserting additional vias does not improve the impedance matching. In reality, the physical length of TSVs is electrically short for this frequency range with negligible reflection loss, and hence there is no critical need to match the impedance. But at higher frequencies where the EM mode is dielectric TEM mode, optimizing the pitch between the signal via and the ground vias can improve the impedance matching.

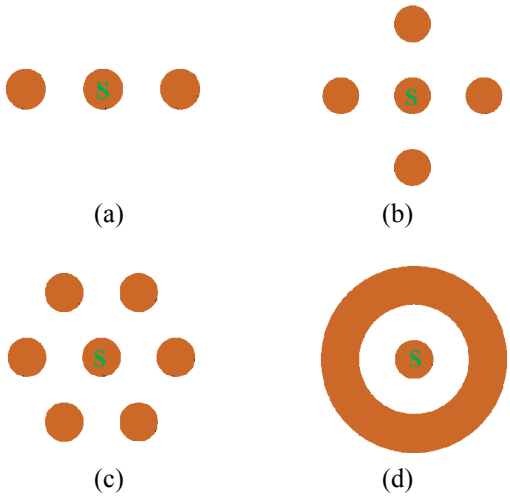


Figure 6. Four via configurations: (a) two ground vias adjacent to a signal via, 2G1S or GSG; (b) four ground vias with a signal via, 4G1S; (c) six ground vias with a signal via, 6G1S; (d) coaxial via.

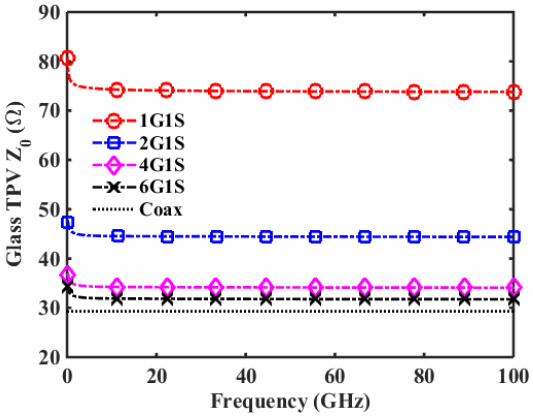


Figure 9. Impedance as a function of frequency for various TPV configurations in glass.

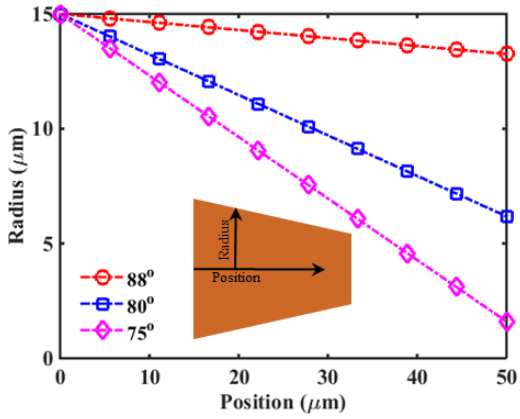


Figure 10. TPV radius varies along TPV length from top to bottom in glass.

In contrast, the impedances of various via configurations in intrinsic silicon and glass are similar to each other, but different from those in lossy silicon. The results depicted in Fig. 8 and Fig. 9 show the effectiveness of inserting additional ground vias in reducing the impedance mismatch. In Fig. 8, by introducing an extra ground via to the GS configuration at minimum pitch, namely the GSG configuration, the impedance drops to 31 Ω, and continuously adding ground vias brings down the impedance closer to that of the coaxial via in Fig. 6 (d). A similar behavior was observed for TPVs in glass in Fig. 9. Thus, it can be concluded that adding ground vias is an efficient way to reduce the impedance, and if 50 Ω matching is desired, the pitch between the signal via and the ground vias needs to be optimized.

IV. Effect of Via Taper

Unlike TSVs in silicon, TPVs in glass have a tapered shape [3, 4], and depending on the via formation method used, the taper angle can vary from 75° to 88°. Based on the assumption that vias are linearly tapered, this section studies the effect of via taper on the impedance and the S-parameters.

A. Impedance

Geometrically, the taper gradually shrinks via radius along the length of the via, as illustrated in Fig. 10. The via radius was assumed to be 15 μm on top, and different taper angles resulted in different taper slopes. For the best-reported taper angle in the literature till date of 88°, the bottom radius was 13.25 μm, which is close to the 15 μm radius at the top; but for the worst taper angle (75°), the bottom radius was 1.60 μm, which is significantly smaller than the 15 μm radius at the top. Hence, taper has a significant impact on the via opening, especially the bottom opening.

When the via length is comparable to the wavelength of the operation frequency, the linearly tapered radius causes different impedances along the via length. Fig. 11 shows the impedance of a 30 μm diameter signal TPV adjacent to a 30 μm diameter ground TPV along TPV length, for 88°, 80° and 75° taper angles in glass. The impedances simulated by 3D EM solver matched well with those computed by equation (1). It can be seen that for the best-reported 88° taper angle and for the 80° taper angle, the impedance almost linearly increases along the TPV length with a maximum impedance increase of about 10% at the bottom, while for the worst case of 75° taper angle, the impedance increase rate becomes much higher as the wave approaches the bottom of vias. Although this study was performed for TPVs in glass, similar conclusions can be made for TSVs in lossy and intrinsic

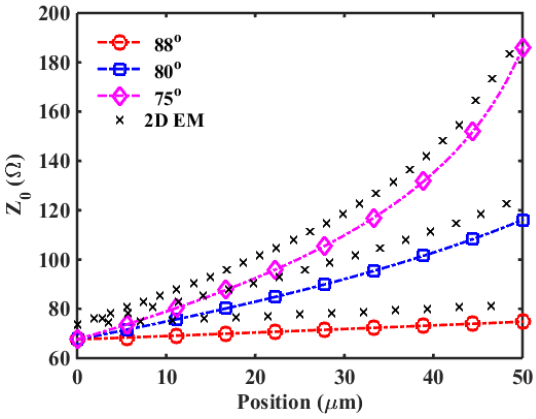


Figure 11. TPV impedance varies along TPV length from top to bottom in glass.

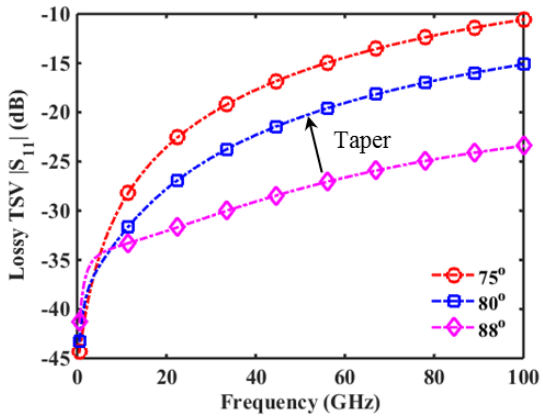


Figure 12. S_{11} Magnitude as a function of frequency for 75°, 80° and 85° tapered TSVs in lossy silicon.

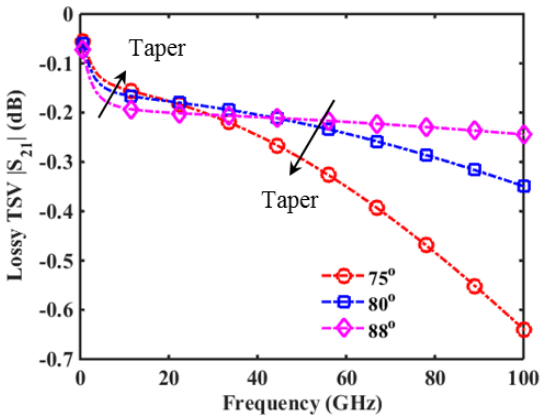


Figure 13. S_{21} Magnitude as a function of frequency for 75°, 80° and 85° tapered TSVs in lossy silicon.

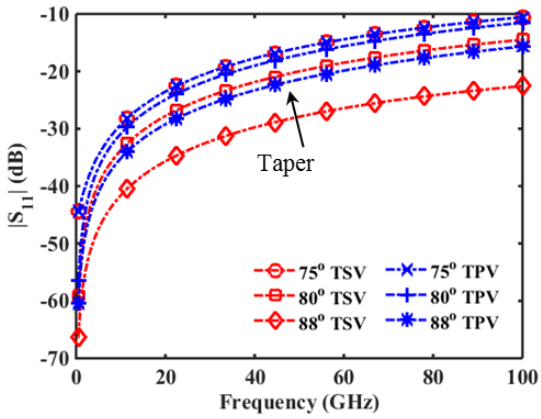


Figure 14. S_{11} Magnitude as a function of frequency for 75°, 80° and 85° tapered TSVs in intrinsic silicon and TPVs in glass.

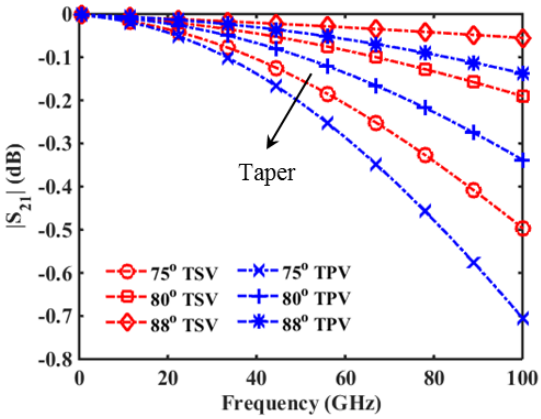


Figure 15. S_{21} Magnitude as a function of frequency for 75°, 80° and 85° tapered TSVs in intrinsic silicon and TPVs in glass.

silicon.

B. S-Parameters

In addition to the impedance, the S-parameters were simulated from 0.1 GHz to 100 GHz for the scenario of GS vias in lossy silicon, intrinsic silicon and glass. The magnitude of S_{11} and S_{21} for GS TSVs in lossy silicon are shown in Fig. 12 and Fig. 13, respectively. From Fig. 12, it can be seen that TSVs with increasing taper have stronger reflections. This is because the via taper increases the self-inductance, worsening the impedance mismatch between GS TSVs and the 50 Ω terminations. On the other hand, the S_{21} values in Fig. 13 indicate that the taper has a positive impact below 20 GHz, which is consistent with the conclusion in [8], but it has a negative impact above 40 GHz. The reason for this is the transition in the EM mode. Below 20 GHz when the slow-wave mode is excited, the capacitance of the SiO_2 liner is reduced because of the taper; above 40 GHz when the dielectric TEM mode is excited, the loss from copper and the silicon substrate increases as TSVs become more tapered. Thus, we can conclude that TSV taper improves the performance below 20 GHz but degenerates the performance above 40 GHz.

Similar analysis was performed for TSVs in intrinsic silicon and TPVs in glass. The behavior in each of these cases was similar, but different from that of TSVs in lossy silicon. The magnitude of S_{11} in Fig. 14 shows that as vias get more tapered, the reflection increases, which is attributed to the increase in inductance with taper. From the magnitude of S_{21} in Fig. 15, it can be seen that increasing via taper results in higher loss. There are two reasons for this behavior, namely: 1) more tapered vias have larger inductance, resulting in more reflection loss; and 2) more tapered vias have smaller openings and less copper to conduct current. Hence, we can conclude that via taper has a negative impact on performance for TSVs in intrinsic silicon and TPVs in glass at all frequencies.

V. CONCLUSIONS

This paper presents one of the first comprehensive studies comparing the electrical behavior of TSVs in silicon with TPVs in glass in many areas including the electromagnetic field distribution, design for 50 Ω impedance, and the effect of via taper. There are three modes that exist in TSVs, namely slow-wave mode, dielectric quasi-TEM mode, and skin-effect mode. However, in glass TPVs, only the TEM mode exists, resulting in glass TPVs having lower loss than TSVs in silicon. Based on the 3D EM solver simulation results, the impedance of ground-signal vias was higher than the widely used 50 Ω, and such an impedance mismatch can be improved by introducing multiple ground vias in close proximity to the signal via. However, adding ground vias does not improve the impedance matching for TSVs in lossy silicon at low frequencies. It was also found that the via taper had a positive effect on TSVs in lossy silicon below 20 GHz, but had a negative effect on TSVs in lossy silicon above 40 GHz. For the TSVs in intrinsic silicon and TPVs in glass, via taper had a negative effect in performance at all frequencies. The results presented in this paper serve as a quick reference for electrical design engineers in designing vias in silicon and glass interposers, considering the effect of via taper.

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