# Design and Demonstration of Ultra-thin Glass 3D IPD Diplexers

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***Abstract*—This paper demonstrates, for the first time, 3D integrated passive device (IPD) diplexers on ultra-thin glass substrates for wireless local area network (WLAN) application in mobile devices. The designed LC-based diplexer was composed of a low-band filter and a high-band filter, built on ultra-thin glass substrates. The two filters were designed on each side of the glass substrate and interconnected by through-package-vias (TPVs) to form a 3D IPD. Ultra-thin and low-loss dryfilm dielectrics were utilized for improved electrical performance as well as to achieve high-density of passives integration. The demonstrated 3D IPD diplexer is 3-4X thinner than current LTCC devices, with lateral dimensions of 1.1mm x 1.3mm in a thickness of 200µm resulting in a low insertion loss of less than 1dB for pass bands and more than 24dB stop-band rejection.**

***Keywords-RF diplexer; glass substrate; thinfilm; TPV; embedded matching network; WLAN***

## I. INTRODUCTION

Low temperature co-fired (LTCC) substrates and surface acoustic wave (SAW) filters are the mainstream radio frequency (RF) components in the market, providing low loss and high quality factor [1][2]. However, they are limited in thickness reduction and large parasitic effects leading to interconnection losses. Traditional organic substrates with large-scale manufacturability can also be considered but fall short in meeting the performance requirements such as precision impedance matching, dielectric and surface losses. To overcome these limitations, Georgia Tech has been pioneering advances in component miniaturization and improved properties utilizing a unique 3D package integration architecture called 3D IPD that adds other advantages at module level. The concept of 3D IPD on glass substrates stands out to overcome the shortcomings of existing technologies, by offering the highest density of passive component integration as well as achieving low loss at a low cost [3], enabled by advanced glass substrate technologies.

The concept of glass-based 3D IPDs involves three major innovations: 1) innovative filter designs with thinfilm LC networks, 2) double-side integration of thinfilm passives on ultrathin glass substrates with through-vias [4] with precision and tolerance, and 3) large-area and low-cost panel processes. These 3D IPDs show 3-4X reduction in thickness with same or better performance compared to state-of-the-art.

The 3D IPD concept can also be extended to 3D integrated passive and active component (IPAC) modules with double-side assembly of active and passive components. RF components, such as RF ICs and filters, can be integrated onto the glass platform with double-side components to form high-density modules with superior performance profiting from ultra-short interconnections and low-loss glass substrates, as shown in Fig. 1. Passives such as 3D IPD diplexers, however, can also be individually fabricated as discrete components, that can then be assembled onto the 3D IPAC glass substrates, or be integrated as embedded passives. RF modules [3] with 3D IPAC concept are projected to bring unprecedented performance and size benefits for WLAN, LTE, 5G and millimeter wave applications.

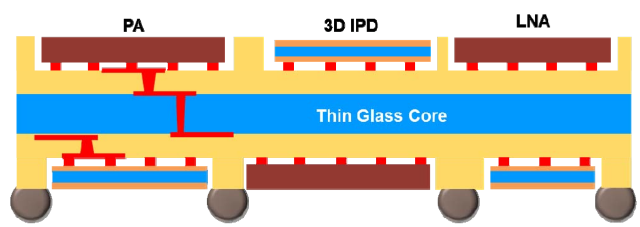



Figure 1. Concept of glass 3D IPAC RF Module.

This paper focuses on the modeling, design, fabrication and demonstration of 200µm thick ultra-miniaturized glass 3D IPD diplexers, as shown in Fig. 2, with advances in glass technologies.

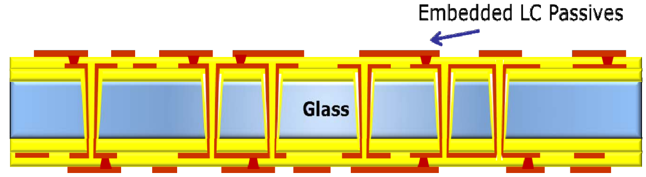



Figure 2. Concept of glass 3D IPD diplexer.

The designed diplexer was composed of a low-pass filter (LPF) for low-frequency band and a high band-pass filter (BPF) for high-frequency band. Embedded lumped inductors and capacitors were used to build these filters. Therefore, a full electromagnetic (EM) simulation of 3D structure was

978-1-5090-1204-6/16 $31.00 © 2016 IEEE
DOI 10.1109/ECTC.2016.265

conducted. The diplexer was designed targeting a insertion loss of less than 1dB, return loss more than 10dB, for both high-band and low-band paths, and more than 24dB for out-of-band attenuation.

Ultra-thin 100µm glass substrates with low loss and ultra-thin build-up dielectric films were utilized to form the glass substrate. These thinfilm dielectrics were laminated on both sides to form 3D embedded passives. High-band filter was built on top side of the glass substrate while low-band filter was built on the bottom side. They were connected by TPVs with short interconnection lengths. Each of the two filters occupied two metal layers (ML) in a 2+0+2 stack configuration. The availability of fine line re-distribution layer (RDL) technologies with thinfilms on glass substrates resulted in the size shrinkage of lumped elements so that the 3D IPD diplexer could be miniaturized both horizontally and vertically. The line width precision was well controlled by precise lithography with ultra-thin high-resolution photoresists and advanced semi-additive processes (SAP) for metallization [5].

First part of this paper covers the design and 3D EM simulation of the 3D IPD diplexers on glass, targeting design metrics for both electrical performance and dimensions.

The second part of this paper focuses on process development with ultra-thin glass towards the 3D IPD diplexer demonstration. Low-cost and reliable TPV formation and advanced RDL metallization for precise line formation are discussed.

The last session of this paper presents the characterization of the demonstrator using 3D microscopy. Process variations in terms of linewidth, polymer thickness and copper thickness are measured and compared with design.

## II. DEISIGN AND SIMULATION

The stack-up of the ultra-thin glass substrate is shown in Fig. 3. A 100µm thin glass was chosen as the core material, which has a dielectric constant of 6.7 and loss tangent of 0.004. Low-loss 15µm dry film polymer was applied on both sides of the glass as inner primer layers as well as build-up dielectrics. Detailed substrate design parameters are provided in Table 1.

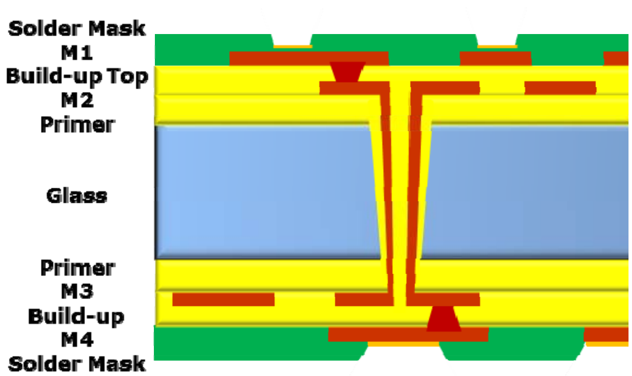



Figure 3. Substrate geometry of modeled 3D IPD diplexer.

TABLE I. SUBSTRATE DESIGN PARAMETERS

| Substrate Stack-up | | |
|---|---|---|
| ***Items*** | | ***Thickness (µm)*** |
| ***High-band Filter*** | Solder Mask (Top) | 15 |
| | M1 | 8 |
| | Build-up (Top) | 15 |
| | M2 | 8 |
| | Primer (Top) | 15 |
| ***TPV*** | Glass Core | 100 |
| ***Low-band Filter*** | Primer (Bottom) | 15 |
| | M3 | 8 |
| | Build-up (Bottom) | 15 |
| | M4 | 8 |
| | Solder mask | 15 |
| **Design Rules** | | |
| ***Items*** | | ***Size (µm)*** |
| TPV | | 100 |
| Blind Via | | 45 |
| Min L/S | | 15 / 15 |

The circuit-level design of diplexer was first conducted in Agilent ADS® to determine the filter design topology. For miniaturization consideration, lumped elements were utilized to build the filters. It was determined that five capacitors and three inductors were required to meet the targeted electrical performance. The circuit was then translated into a 3D model in SONNET® based on proposed substrate design rules. A 3D overview of the model was shown below in Fig. 4.

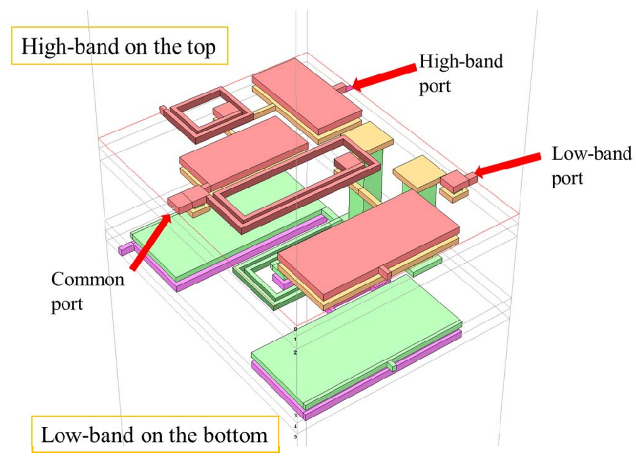
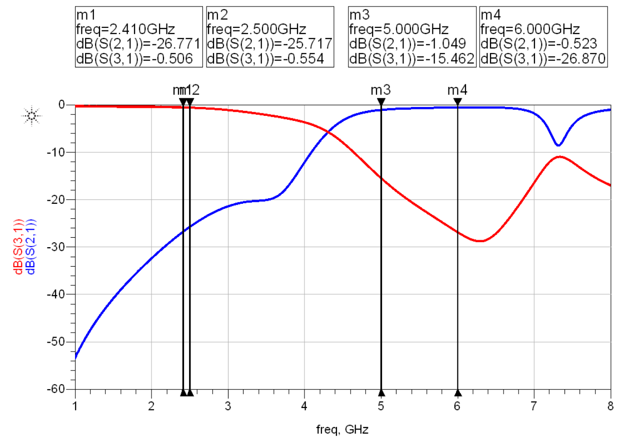


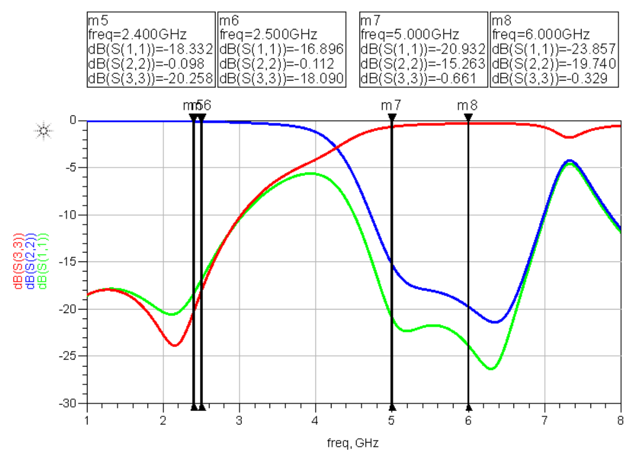

Figure 4. 3D layout of designed diplexer.

High-band band-pass filter and low-band low-pass filter were distributed on either sides of the glass and connected through TPVs. This 3D architecture not only reduced the volume of the component compared with a lateral arrangement, but also benefited the processability and mechanical stability of the substrate due to parallel double-side processing during its fabrication. The X-Y dimensions of this designed 3D IPD diplexer was 1.1 x 1.3mm. For measurement convenience, three sets of ground-signal-ground (GSG) pads were added to each port and were all placed on the topside metal layer M1.

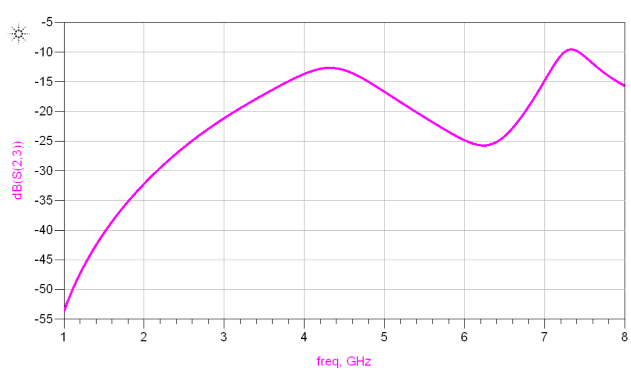
Full-wave EM simulation was conducted from 1GHz up to 8GHz. The simulation results of designed diplexer are below in Fig. 5.




(a)




(b)




(c)

Figure 5. EM simulation results of 3D IPD diplexer: (a) insertion loss of low-band and high-ban paths, (b) return loss at three ports, and (c) isolation.

Less than 1 dB insertion loss was achieved at both low-band path from 2.4GHz to 2.5GHz and high-band path from 5GHz to 6GHz. While the diplexer was operating in the low frequency band, the stopband suppression reached more than 25dB, and in high-band operation, the stopband suppression was more than 15dB. Regarding the return loss, more than 15dB and 18dB had been achieved for low band and high band respectively. The common port was matched so that the return loss at this port was maintained more than 16dB. The port-to-port isolation between two paths was more than 17dB in both bands.

## III. SUBSTRATE FABRICATION

The process flow of glass 3D IPD diplexer fabrication is summarized in Fig. 6.

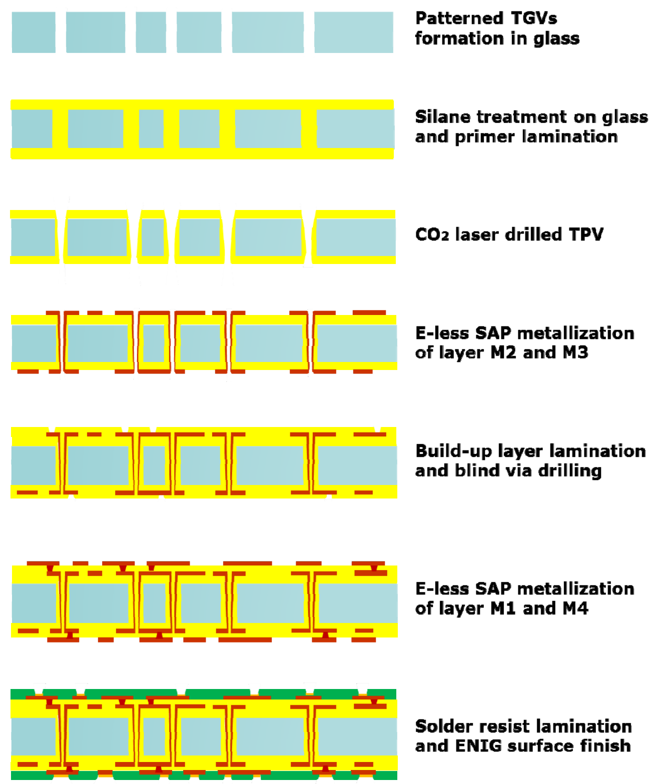



Figure 6. Process flow of glass 3D IPD diplexer fabrication.

Through-glass-vias (TGVs) with 100μm diameter were formed in bare glass as the first step. TGVs could be manufactured through chemical or laser-based approaches [6]. To enhance the handling of ultra-thin glass during fabrication, 15μm thick polymer was laminated onto glass and it provided sufficient volume to flow inside those pre-formed TGVs. Later on, $CO_2$ laser was applied directly on those TGV locations to ablate the polymer filled inside and drill 60~80μm diameter via-in-via TPVs. Since the resulted TPVs have polymer-coated sidewall, conventional SAP processes with electroless-plated copper seed layer could be applied for metallization. The results of via-in-via TPV formation in glass are shown below in Fig. 7.

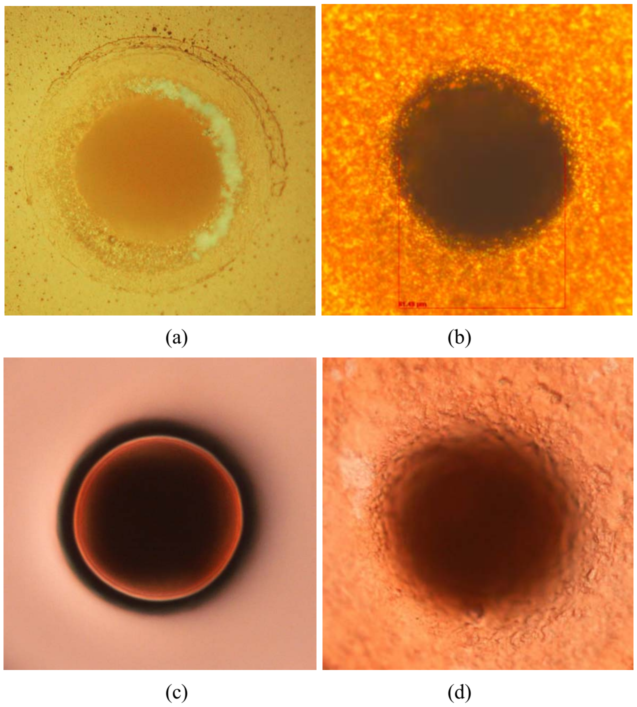



Figure 7. Via-in-via TPV formation process: (a) laser-drilled TPV inside polymer filled TGV, (b) eless seed layer plating inside TPV, (c) TPV metallization by electrolytic plating, and (d) fabricated TPV after seed layer etching.

It was then followed by build-up layer lamination, blind via drilling and metal layers patterning. Cross-sectional view of fabricated 4ML glass substrate with via-in-via TPV integration is shown in Fig. 8.

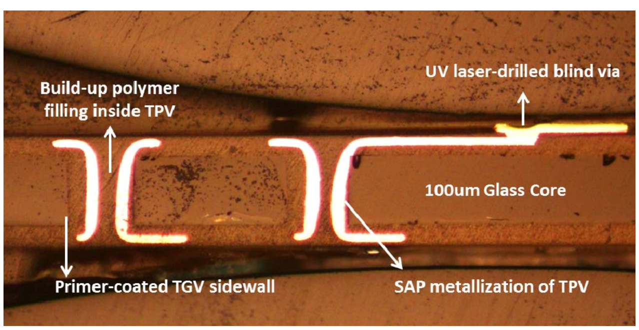



Figure 8. 4ML glass substrate with via-in-via TPVs.

This innovative via-in-via approach benefits the glass panel manufacturing in three ways: 1) ultra-thin glass handling is improved with primer layer 2) electroless plating can be used for copper seed formation to lower the cost and addresses the challenges of direct copper metallization on glass [7]; and 3) serving as a buffer layer, primer effectively relieves the stress at copper and glass interface, where an apparent coefficient of thermal expansion (CTE) mismatch exists, and improves the TPV reliability.

A top view of fabricated diplexer at M1 layer before solder mask lamination and surface finish is shown in Fig. 9.

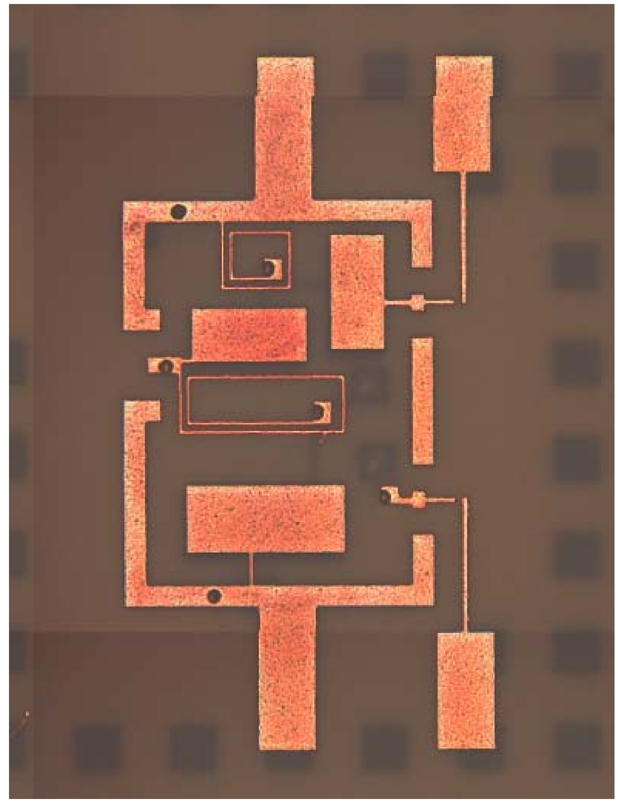


Figure 9. Top view of fabricated diplexer before surface finish.

For this prototype 3D IPD diplexer demonstration, 6'' x 6" glass panel was used, which is further scalable to large size manufacturing. Fig. 10 gives an overview of the first demonstration of 3D IPD diplexer on glass with a 4ML double-side stack and TPV integration.

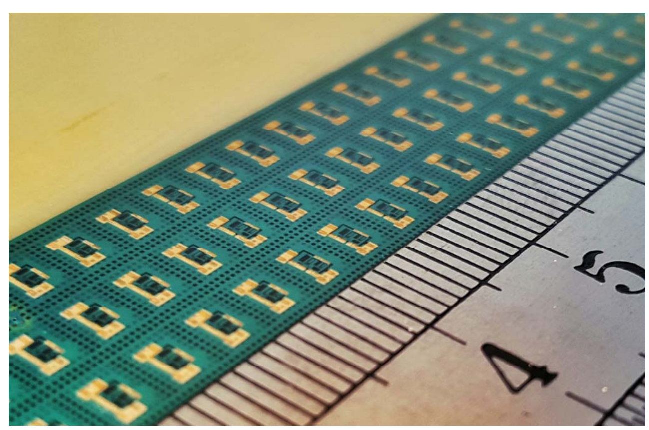


Figure 10. First demonstration of 3D IPD diplexer on glass.

## IV. Measurements

Process variation plays a predominant role in determining RF circuit performance. The lateral dimensional changes of the metal traces are mostly affected by photo lithography and seed layer removal. Utilizing 15µm thin photoresist with sub-5µm structure resolution capability, the variation of trace width of a 15µm line was controlled below 5%. However, the metal traces presented a trapezoidal shape at the cross-section. This tapper effect of the metal on the surface was a result of sidewall etching during isotropic seed layer removal process, and was quantified as 3µm in average for each layer. When it comes to the thickness variation, without any metal planarization process presented, the measured variation of copper thickness was 1.5µm. Since ultra-thin 15µm polymer was applied in this study, its thickness on the copper was also correlated to the variation of copper metallization. Consequently, the glass 3D IPD diplexer showed an improved process-to-design validation compared with prevalent packaging technologies at small design features and miniaturized substrate profile.

## V. ACKNOWLEDGEMENT

The authors would like to thank Corning Inc. for providing the glass substrates for this research and Gigalane Co., Ltd. for funding the project. The authors would also like to thank GT-PRC RDL research team for their technical guidance on glass substrate fabrication.

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