Scaling Cu pillars to 20um pitch and below: critical role of surface finish and barrier layers

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***Abstract*— High-performance computing has been aggressively driving pitch and performance requirements for off-chip interconnections over the last several decades, pushing solder-based interconnections to their limits. The most leading-edge Cu pillar technology faces many fundamental challenges in scaling to pitches below 30um, in particular with stress management and increased risks of Au embrittlement as solder volume is reduced All-intermetallic interconnections formed by solid-liquid interdiffusion (SLID) bonding have been concurrently explored to extend solders to finer pitches and improve their performance, but face their own set of manufacturability and reliability challenges that have, so far, limited their use to 3D-ICs. This research comprehensively addresses these challenges with innovative interconnection designs and advances in surface finish metallurgies, which allow for precisely controlled and unique interfacial reactions. A two-fold approach is pursued to: 1) extend scalability of conventional Cu pillars by replacing standard ENEPIG with ultra-thin electroless Pd autocatalytic Au (EPAG) surface finish; and, for further pitch scaling and enhanced electrical and thermal performances, 2) enable void-free, manufacturable all-intermetallic joints solely composed of the metastable Cu_6Sn_5 phase by introduction of diffusion barrier layers. This paper presents the design, demonstration and characterization of such high-performance solder-based interconnections at 20um pitch, highlighting the strategic role of surface finish and diffusion barrier layers for potential further pitch scaling.**

Keywords-Cu pillar interconnections, flip-chip thermo-compression, metastable SLID bonding, interfacial reactions, diffusion barrier layers, surface finish metallurgy

I. INTRODUCTION

High-performance computing has been aggressively driving the need for higher I/O densities to meet its increasing system bandwidth requirements. Advances in packaging technologies such as high-density 2.5D interposers have recently been introduced to enable high-speed, high-bandwidth die-to-die communication, for instance between logic and memory dies. This new approach to system design following the "die split" trend requires scaling of chip-to-substrate (C2S) interconnections, with pitches projected to reach down to 20µm by 2020 according to the ITRS roadmap. The Cu pillar technology has recently emerged as the technology of choice for fine-pitch applications, and been demonstrated at pitches down to 40µm in mass production and 30µm in R&D. However, Cu pillar interconnections face several fundamental limitations hindering further scaling [1].

Pitch scaling is accompanied by a reduction in solder volume to prevent bridging. While the typical solder height is of 15-30µm in today's Cu pillars, it is expected to shrink to less than 10µm in 20µm-pitch interconnections. With this trend, intermetallics start contributing more significantly, to the point of eventually dominating the overall joints' composition, properties and reliability. With such limited solder volume, severe mechanical stresses can build up at the interface between residual solder and intermetallics to the level where they can potentially create micro-cracks right after assembly, eventually leading to joint failures. Further, high-performance substrates typically use surface finish metallurgies with Au and Pd thin-film layers such as ENIG or ENEPIG, to control intermetallic formation and improve solder wettability. At fine pitch, the volumetric contribution of Au and Pd in solder increases, aggravating risks of Au embrittlement and resulting interconnection failures [2, 3]. Precise control of interfacial reactions has, therefore, become a major fundamental bottleneck to achieving reliable solder-based interconnections at ultra-fine-pitch.

In addition to the aforementioned reliability concerns, Cu pillar scaling is also inherently limited by the physical properties of solders. Reduced interconnection diameters at fine pitch results in increasing current densities of $10^5 A/cm^2$ and above, far exceeding the power-handling capability of Sn-based solder alloys. Increasing power densities in high-performance computing predicted by the ITRS roadmap, from $0.45W/mm^2$ in 2009 to a projected $1.15W/mm^2$ by 2020, also bring a significant rise in operating temperatures, up to 100°C, near half the melting point of standard lead-free alloys beyond which creep effects become extremely damaging to thermomechanical reliability.

All-intermetallic interconnections formed by solid-liquid interdiffusion (SLID) bonding have been proposed to address this performance gap while retaining the ease of

processability and low cost of solders. SLID bonding comes as a natural evolution of Cu pillars at fine pitch as full conversion to intermetallics is almost unavoidable with such fine amounts of solder if not during chip-level assembly, then during subsequent process steps. Intermetallics have high melting points giving high thermal stability and superior electromigration performance than solders [4]. SLID bonding has been demonstrated at pitches of 10-20µm in 3D-IC Si-Si bonding, but faces many challenges for use in C2S applications, including long assembly cycle times, non-standard and costly bumping processes, and void formation degrading electrical, thermal and reliability performances [5, 6]. A new metallurgical system is thus required to enable void-free intermetallic joints with improved bumping and assembly manufacturability and extend applicability of SLID bonding to C2S assemblies.

To address the aforementioned critical needs, the Georgia Tech Packaging Research Center and its industry partners pioneered a new class of solder-based interconnection technologies with pitch scalability below 20µm, standoff height below 15µm, thermal stability at 200°C and power handling capability up to 10^5A/cm^2. This is achieved by design of new interconnection systems for precise control of interfacial reactions, using advanced surface finish materials and barrier layer designs to 1) scale the conventional Cu pillar technology to 20µm pitch with a solder height of less than 10µm; and 2) demonstrate manufacturable, void-free SLID interconnections at 20µm pitch with power-handling capability and thermal stability beyond that of standard solder-based technologies.

The Cu pillar interconnection system was first redesigned with introduction of a new surface finish metallurgy, EPAG by Atotech GmbH, to replace standard ENEPIG. Elimination of Ni diffusion barrier layers in the interconnection system is suggested to mitigate risks of Au embrittlement and enable reliable Cu pillar interconnections with reduced solder volume. The EPAG composition was previously optimized for Cu pillars with less than 7µm solder height, scalable to 20µm pitch, based on the study of interfacial reactions through high-temperature storage (HTS) at 200ºC, as detailed in [7]. This paper goes beyond with a comprehensive study of the effect of surface finish metallurgy on the microstructure and reliability performance of standard Cu pillar joints as well as Cu pillars with reduced solder volume, with consideration of Cu consumption from the substrate trace. Results are summarized in section II.

Further, a new SLID interconnection design was recently proposed to form void-free interfaces with improved electrical, thermal and reliability performances as well as enhanced manufacturability [8]. This new concept relies on the introduction of Ni barrier layers to isolate the metastable Cu_6Sn_5 phase and prevent further evolution to the stable Cu_3Sn phase, targeted in standard SLID approaches. This technology benefits from the following advantages: 1) liquid-phase reaction for full conversion to intermetallics in less than a minute; 2) no voiding due to formation of a single intermetallic phase, Cu_6Sn_5, and its low volume shrinkage; and 3) bumping materials and processes compatible with existing infrastructures. Design of the interconnection stack-up based on theoretical diffusion, kinetics and thermomechanical modeling is presented in section III with considerations of bumping and assembly manufacturability. This technology achieved outstanding electromigration performance, thermal stability at high temperatures and superior thermomechanical reliability and is demonstrated, for the first time, at 20µm pitch on silicon and glass substrates.

II. Copper Pillar Scaling

Scaling of the Cu pillar technology to pitches below 30µm requires a reduction in solder height to less than 10µm with unprecedented microstructural challenges, such as Au/Pd embrittlement and increased interfacial stresses. A revisit of the Cu pillar metallurgical system is required to address these challenges and finely control intermetallics formation.

A. The Barrier Layer Debate

In conventional Cu pillar interconnections, a Ni barrier layer, 2-3µm in thickness, is typically introduced between Cu pillar and solder cap to prevent solder from directly reacting with Cu and inhibit Cu consumption from the Cu pillar. Similarly, the thick Ni layer present in standard ENIG or ENEPIG blocks diffusion of solder to the Cu trace on substrate side. With the trend to thinning the wiring thickness in high-density substrates such as 2.5D interposers, limiting Cu consumption from the trace may seem critical. However, the presence of such diffusion barrier layers aggravates risks of Au embrittlement. Despite its prohibitive cost, Au has been favored as reacting layer in surface finishes used in high-performance applications for its superior solder wettability. However, the high dissolution rate of Au in Sn may result in formation of brittle Au-Sn intermetallics, so-called Au embrittlement, degrading the joints' shear strength and thermomechanical reliability.

The golden rule to prevent Au embrittlement is to limit the concentration of Au in Sn to below 0.1wt.%. As the solder height scales with pitch, the volumetric concentration of Au in Sn increases. Massive formation of $(Au,Pd,Ni)Sn_4$ intermetallic has already been reported in [2] after 200h of HTS for conventional Cu pillar interconnections with 20µm solder height. At 20µm pitch, reduced solder height to below 10µm caps the Au thickness to 4nm to eliminate any risks of Au embrittlement. Achieving such low Au thickness in surface finish processing is unrealistic given production constraints and the need for acceptable shelf life of substrates. With elimination of Ni barrier layers, Sn would react directly with Cu, resulting in formation of the metastable Cu_6Sn_5 phase. Owing to the 24.3at.% Au solubility of $(Cu,Au)_6Sn_5$, a 4µm-thick layer of $(Cu,Au)_6Sn_5$ can now accommodate up to 85nm of Au without any risk of embrittlement, significantly more compatible with manufacturing process tolerances.

While Ni- and Au-free surface finish metallurgies already exist, such as immersion Sn (ImSn), immersion Ag (ImAg) or organic solderability preservatives (OSP), they do not meet performance and reliability requirements of fine-pitch interconnections [9-12]. The new EPAG surface finish was

recently developed by Atotech GmbH. This ultra-thin, Ni-free surface finish can be applied on substrate interconnects at less than 10µm pitch without any extraneous plating [13]. Further, as wettability is dominated by the first layer solder reacts with, the Au layer, EPAG showed excellent solderability, comparable to that of ENEPIG [7]. To demonstrate EPAG as a new surface finish technology with superior resistance to Au embrittlement, Cu pillar interconnections were assembled on EPAG with the various compositions reported in Table I. Standard ENEPIG with Ni 4µm Ni/50 nm Pd/Au 50nm was used as benchmark.

TABLE I. EXPERIMENTAL PLAN FOR EVALUATION OF EPAG SURFACE FINISH

EPAG composition	Pd thickness (nm)	Au thickness (nm)
EPAG-A	50	50
EPAG-B	100	50
EPAG-C	100	100
EPAG-D	150	50

B. *Test Vehicle Designs*

Two daisy-chain test vehicle designs were considered in this study, as shown in Fig. 1. The first test vehicle, provided by WALTS Co., LTD, consists of a Si test die with conventional 554 Cu pillar interconnections in a single peripheral row at 50µm pitch. The Cu pillars consist of pre-reflowed 30µm Cu microbump, a 2µm Ni barrier layer, and a 15µm solder cap. The second test vehicle consists of a Si test die with 760 I/Os arranged in 3 peripheral rows at 100µm inline pitch, and a central area array at 250µm pitch. The test dies were bumped with the ultra-short Cu pillars shown with 10µm Cu microbumps and 10µm solder caps. These design rules were selected for their scalability to 20µm pitch. The interconnections were not pre-reflowed to prevent excessive intermetallic formation, and, therefore, lack the typical dome shape observed in conventional Cu pillars.

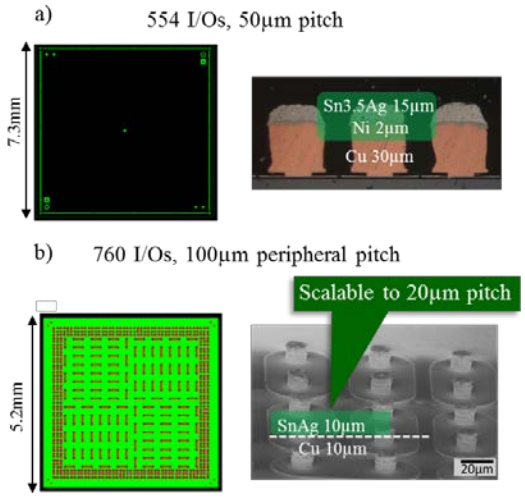

Figure 1. Test vehicle designs with a) standard Cu pillars, and b) ultra-short Cu pillars with reduced solder height.

Simple one-metal-layer organic substrates were used with surface finish applied on Cu traces and pads by Atotech GmbH with accurate composition control. Assembly was performed by standard thermocompression bonding with non-conductive paste (TC-NCP) provided by Namics Corporation.

C. *Interfacial Reactions and Thermomechanical Reliability*

Assemblies with standard Cu pillars with Ni barrier layer were subjected to 500h of HTS at 150°C to study interfacial reactions with ENEPIG and EPAG surface finishes. Results from SEM/XEDS cross-sectional analysis are displayed in Fig. 2. After bonding, Au embrittlement could already be observed in joints assembled with ENEPIG and EPAG-B/C/D with dominant $(Pd,Au,Ni)Sn_4$ and $(Pd,Au)Sn_4$ intermetallics, respectively. Only with EPAG-A was Au embrittlement effectively prevented, with formation of $(Cu,Ni)_6Sn_5$. As Pd also contributes to Au embrittlement, these findings are in good accordance with the design recommendations provided in section II-A.

After HTS, the ENEPIG joints were found solely composed of brittle $(Pd,Au,Ni)Sn_4$, with significant shrinkage and micro-cracks. With all EPAG compositions, massive Cu-Sn intermetallic growth was observed with scarce $(Pd,Au)Sn_4$. These results indicate that EPAG surface finish can significantly reduce risks of Au embrittlement in conventional Cu pillar interconnections, and subsequently, improve thermomechanical reliability.

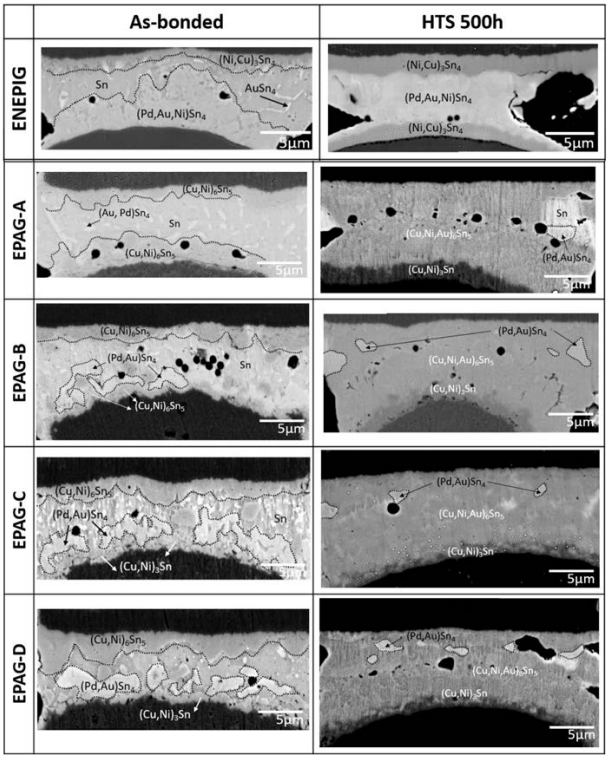

Figure 2. Interfacial characterization of assemblies with standard Cu pillars through 500h HTS at 150°C.

Assemblies were subjected to thermal shock at -55°C/ 125°C with two cycles per hour following JEDEC JESD22-A113F standard. Early failures occurred with ENEPIG with 10% of the daisy chains failing after only 400 cycles, and only ~80% of the daisy-chains surviving the required 1000 cycles. Over 90% of the daisy-chains passed 1000 cycles without failures with EPAG. EPAG-A performed the best with 95% survival rate. These results were expected in regard of as-bonded compositions, with Au embrittlement degrading reliability with ENEPIG.

Detailed interfacial characterization of assemblies with reduced solder volume and no barrier layer was reported in [7]. Results were similar as with standard Cu pillars for ENEPIG, with formation of a thick layer of $(Au,Pd,Ni)Sn_4$ during assembly, subsequently acting as a diffusion barrier layer leading to a phase transformation as shown in Fig. 3. However, a unique reaction was observed in the case of EPAG-A with formation of the single $(Cu,Pd)_6Sn_5$ phase stabilizing the microstructure. As expected, ENEPIG assemblies exhibited poor thermomechanical reliability with 80% of daisy chains failed after only 100 thermal shock cycles, while over 80% of the daisy-chains passed with stable resistances with EPAG-A. This EPAG composition with 50nm Pd/50nm Au is thus the most promising surface finish to achieve reliable Cu pillar interconnections at ultra-fine pitch. However, in absence of a diffusion barrier layer on substrate side, solder reacts directly with Cu, thinning down the Cu traces. It is, therefore, critical to quantify the expected Cu consumption occurring both during assembly through a liquid-state reaction and during 500h HTS through a solid-state reaction.

D. Cu Trace Consumption with EPAG Surface Finish

The initial thickness of Cu traces was measured using 3D confocal microscopy, while SEM measurements were used to determine their thicknesses after assembly and HTS from cross-sections, as illustrated in Fig. 4. With the optimal EPAG-A composition, ~0.6µm of Cu was consumed during assembly compared to 0.07µm with ENEPIG. Diffusion models for solid-state intermetallic growth were used to predict a 2.6µm Cu consumption with EPAG-A after 500h HTS, in good accordance with experimental results. Only 0.16µm of Cu was consumed in the case of ENEPIG.

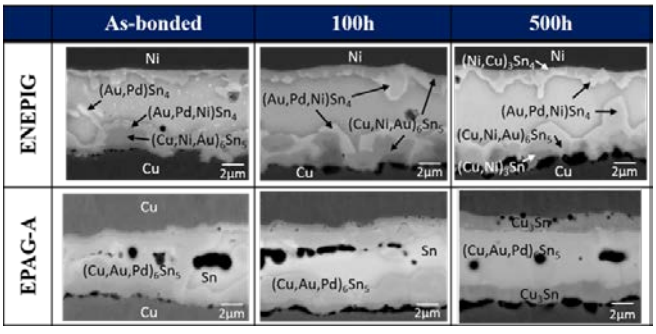

Figure 3. Interfacial characterization of assemblies with ultra-short Cu pillars without barrier layer through 500h HTS at 150°C.

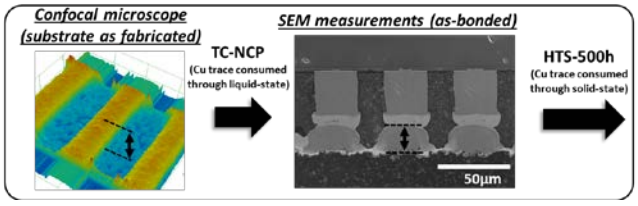

Figure 4. Method for quantification of Cu consumption from the substrate traces.

E. Conclusions

Scalability of the Cu pillar technology to 20µm pitch was demonstrated with a novel metallurgical system consisting of non-reflowed, Ni-free Cu pillar interconnections with solder caps less than 10µm in height, and a 50nmPd/50nmAu surface metallurgy applied on substrate pads. In absence of barrier layers, Cu consumption from the Cu pillars and substrate traces is to be expected. A minimum trace thickness of 5µm is recommended to maintain good adhesion to the substrate and mitigate interfacial stresses. While the shift to non-reflowed bumps may aggravate filler entrapment from the NCP material, the projected move to wafer-level non-conductive films should fully address this challenge.

The proposed interconnection system can achieve the targeted I/O pitch, but cannot meet the increasing power handling, thermal stability and thermomechanical reliability requirements of future high-performance systems. In addition, further pitch scaling to below 20µm is limited in absence of diffusion barrier layers. Solder would then fully react and form all-intermetallic joints composed of dual Cu_6Sn_5 and Cu_3Sn phases with unavoidable void formation degrading performance and reliability. The metastable SLID bonding technology was proposed to comprehensively address these remaining challenges with intermetallic interconnections designed from first principles to meet emerging pitch, performance and reliability requirements.

III. METASTABLE SLID BONDING

The metastable SLID concept is illustrated in Fig. 5. It relies on the introduction of Ni barrier layers to isolate the metastable Cu_6Sn_5 phase and prevent any further phase transformation. For compatibility with standard fabrication processes, the bump stack-up was kept close to that of standard Cu pillars with alternating layers of Cu/Ni/Cu/Sn while the Ni barrier layer on substrate side is provided by standard ENIG. The bump stack-up and barrier layers were designed based on theoretical diffusion, kinetics and thermomechanical modeling as well as considerations of bumping and assembly manufacturability, as described below.

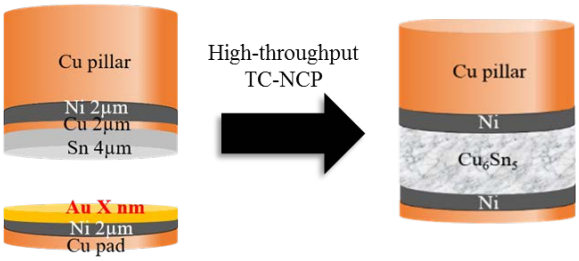

Figure 5. Metastable SLID bonding concept for applicability to chip-to-substrate interconnections.

A. *Design of Interconnection System*

1) Cu-Sn reacting layers: The multilayered CuSn stack was designed to achieve the Cu_6Sn_5 composition, with considerations of bumping and assembly manufacturability. A 2µm Cu thickness and a 4µm Sn thickness were considered. Full transition to Cu_6Sn_5 is expected in less than a minute at 260°C through a liquid-state reaction accelerated by Ni doping from the barrier layers. Due to the wide composition range of $(Cu_{1-x}Ni_x)_6Sn_5$ granted by Cu-Ni substitution, a Cu thickness variation of ~1.2µm from the designed 2µm is acceptable, significantly improving bumping manufacturability.

2) Ni barrier layers: The barrier layers were designed to block the Cu sources from the Cu-Sn reacting layers and prevent formation of Cu_3Sn. As Ni is a highly resistive material and has poor high-frequency performance, the barrier layers should be kept as thin as possible. Based on interdiffusion of Cu and Ni [14], 2800h of annealing at 250°C are required to increase the surface concentration of Cu in 2µm Ni by 1%. Dissolution of the barrier layers under current stressing is another critical design parameter as the driving force for Ni with 10^5A/cm^2 current density is 113X larger than diffusion. Lastly, thermal stability at high temperatures is provided by the high solubility of Ni in $(Cu,Ni)_6Sn_5$ with over 800h of annealing at 260°C required to reach 90% the saturated solubility of Ni in 5µm $(Cu,Ni)_6Sn_5$.

3) Au wetting layer: A 100nm Au thickness yields a ~6.2wt.% Au concentration in 4µm Sn, far greater than the maximum 0.1wt.% recommended to prevent Au embrittlement. However, formation of $(Cu,Au)_6Sn_5$ should be considered. Fig. 6 shows results of assemblies with Au thicknesses varying from 50 to 150nm. Au embrittlement and reduced transition rate were found for 150nm Au, but 100nm Au yielded the targeted reaction and was, therefore, selected to reduce the risks of black pad failures [15, 16].

The metastable bump stack-up was consequently defined as 10µm Cu/2µm Ni/2µm Cu/4µm Sn with ENIG surface finish composed of 2µm Ni and 100nm Au applied on substrate.

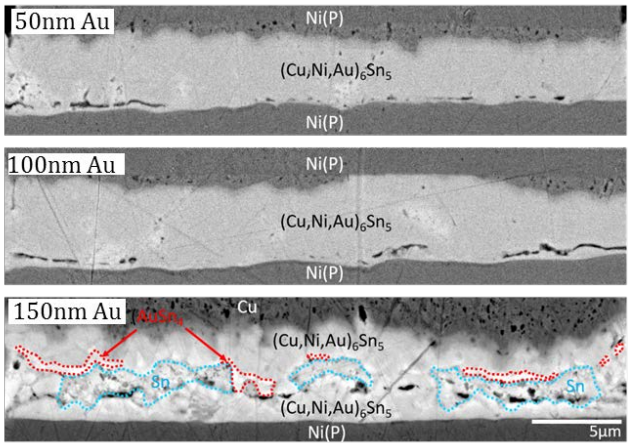

Figure 6. Microstructure of metastable SLID interconnections with varying Au thickness of ENIG surface finish.

B. *Electrical, Thermal and Reliability Performances*

Metastable SLID interconnections were formed by TC-NCP at 260°C with 1min dwell time at peak temperature. Following the design predictions, the joints were solely composed of 5 intermetallic as shown in the SEM/XEDS analysis of the cross-section in Fig. 7. A 2-step assembly where the reaction is initiated in a 3s TC-NCP process and completed through a subsequent reflow step such as board-level SMT was also established to improve assembly throughput [8]. Superior die shear strength of the metastable SLID interconnections has previously been demonstrated, with an average shear strength of ~90MPa, far exceeding that of solders and standard SLID bonding on account of a single intermetallic phase [8].

Preliminary characterization of thermal stability was established through 10X reflow at 260°C peak temperature without further phase transformation [8]. This result was confirmed through 1000h of HTS at 200°C with no dissolution of the Ni barrier layer. As shown in Fig. 8, the joints were still composed of Cu_6Sn_5 with no trace of Cu_3Sn.Entrapment of NCP fillers within the joints is to be noted on the cross-section images.

The metastable SLID interconnections also showed excellent electromigration resistance and survived 1000h of current stressing at 10^5A/cm^2 and 150°C with no voiding or metal dissolution, as illustrated in Fig. 9. The applied current density was an order of magnitude larger than the maximum power handling capability of Sn-based solder alloys.

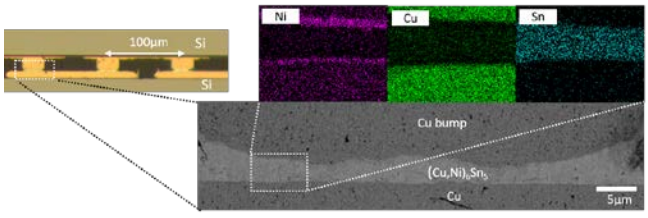

Figure 7. SEM/XEDS analysis of as-bonded metastable SLID joints.

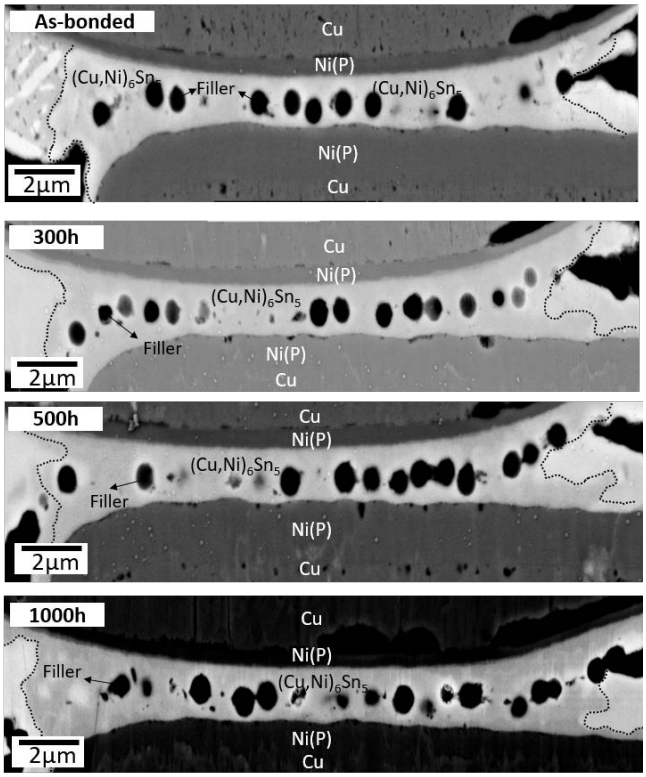

Figure 8. Microstructural evolution of metastable SLID joints through 1000h of HTS at 200°C.

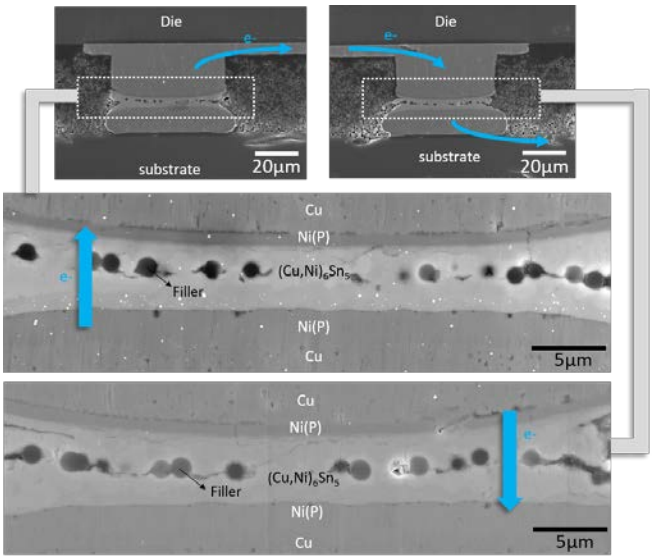

Figure 9. Metastable SLID jonts after 1000h of current stressing at 10^5A/cm^2, 150°C.

Thermomechanical reliability was also evaluated through thermal shock at -55°C/125°C with 2 cycles/h. All but 2 daisy-chains survived over 2000 cycles. The 2 open daisy-chains failed between 500 and 1000 cycles due to excessive NCP filler entrapment acting as pre-cracks. With such stiff intermetallic-based interconnections, failures are not expected within the joints but in the low-k dielectric layers of the chip. The use of pre-applied underfills should prevent such failure by generating compressive stresses on the ultra-low-k layers, preventing propagation of any existing pre-cracks. Evaluation of thermomechanical reliability with low-k wafers is ongoing.

C. First Demonstration at 20µm Pitch

A new daisy-chain test vehicle was designed for the first demonstration of metastable SLID bonding at 20µm pitch. The Si test die of Fig. 10 contains 860 I/Os distributed in a single peripheral row. The test dies were bumped with the designed metastable SLID interconnections, 8µm in diameter. Silicon and glass substrates with ENIG surface finish were fabricated, as shown in Fig. 11. Assembly was successfully demonstrated by TC-NCP using Kulicke and Soffa C2S APAMA production bonder with excellent alignment accuracy confirmed by X-ray imaging. With full electrical yield. Cross-sections of assemblies on Si and glass are shown in Fig. 12 and 13, respectively. The composition of the joints was confirmed to be Cu_6Sn_5 with a minute amount of unreacted Sn. It is to be noted that filler entrapment was significantly reduced at smaller bump diameters, and should be completely eliminated in TC-NCF.

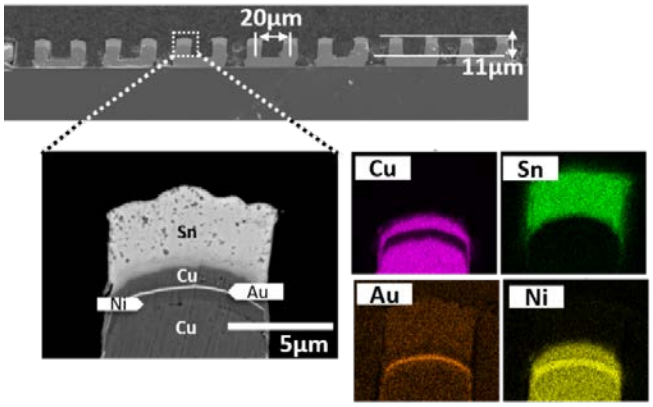

Figure 10. Bumped Si daisy-chain test die at 20µm pitch.

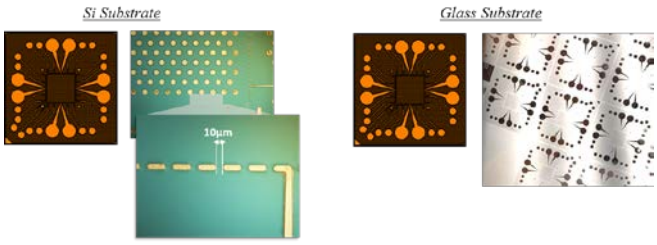

Figure 11. Silicon and glass substrates with metalization at 20µm I/O pitch.

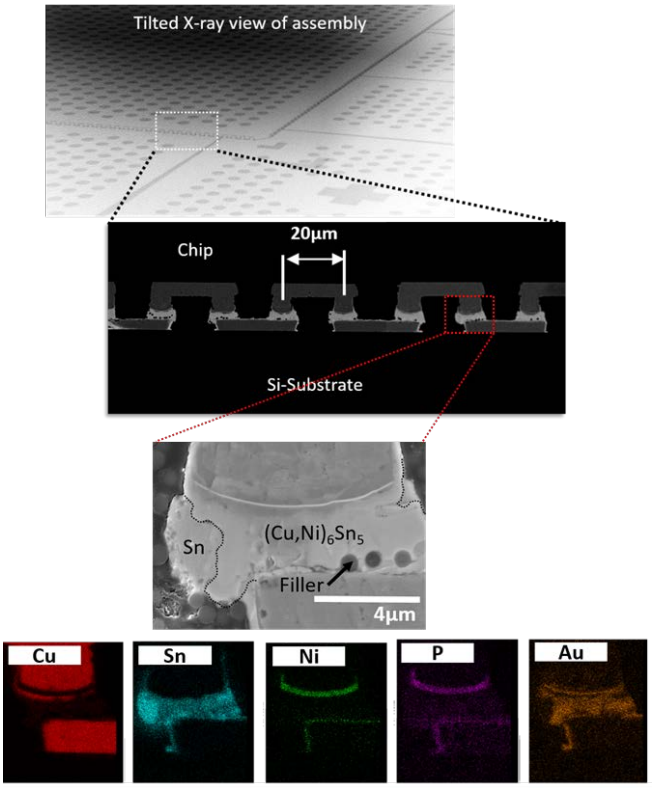

Figure 12. Metastable SLID bonding at 20µm pitch on Si substrate.

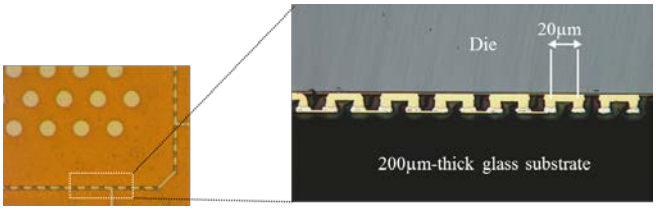

Figure 13. Metastable SLID bonding at 20µm pitch on glass substrate.

IV. Summary and Conclusions

This paper presents the first demonstration of Cu pillar interconnections at 20µm pitch enabled by innovative interconnection designs and advances in surface finish metallurgies, with precisely controlled and unique interfacial reactions. The novel surface finish metallurgy, EPAG was introduced in replacement of standard ENEPIG, limited to coarse wiring pitches due to the conventionally high thickness of its Ni layer. This key innovation, combined to the elimination of both the Ni barrier layer between Cu pillar and solder cap and the pre-reflow step, enabled, for the first time, formation of reliable Cu pillar joints with less than 7µm solder height, scalable to 20µm pitch. The EPAG composition was optimized based on high-temperature storage at 200ºC and detailed study of interfacial reactions through SEM/XEDS analysis. A unique reaction with formation of a single intermetallic phase was observed with a finish composed of 50nm of Pd and Au, yielding joints resistant to Au embrittlement with outstanding thermomechanical reliability.

While Cu pillars may be further scaled in pitch, this does not address their fundamental limitations in terms of electromigration performance and thermal stability. Metastable SLID bonding was demonstrated with improved pitch scalability, electrical, thermal and reliability performances as compared to Cu pillars, as well as enhanced manufacturability compared to standard SLID approaches. This new concept relies on Ni barrier layers designed to isolate the metastable Cu_6Sn_5 phase and prevent further phase transformation to the stable Cu_3Sn phase, targeted in standard SLID approaches. This technology benefits from the following advantages: 1) high bumping manufacturability with large composition range compatible with 300mm-wafer plating tolerances; 2) a 20X reduction in bonding cycle times compared to standard SLID approaches, with a high-throughput 2-step high-speed TC-NCP+reflow assembly; 3) a void-free interface with single intermetallic phase, giving outstanding shear strength of 90MPa; 4) superior power handling capability at 10^5A/cm^2 and 150°C; and 5) thermal stability at temperatures exceeding 200°C. This technology was demonstrated, for the first time, at 20µm pitch on Si and glass substrates.

In summary, this research highlights the strategic role of surface finish and barrier layers in extending pitch scalability of solder interconnections. Novel metallurgical systems are key in enabling better control of interfacial reactions to restore acceptable process windows while improving performance and reliability. The proposed solutions, demonstrated at 20µm pitch, have the potential to be further scaled to meet the needs of tomorrow's high-performance systems following the technology roadmap of Fig. 14.

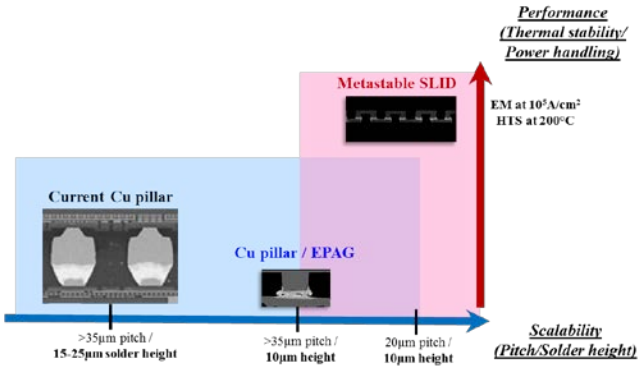

Figure 14. Georgia Tech PRC's roadmap to high-performance, ultra-fine pitch C2S solder-based interconnections.

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