

Via-in-Trench: A Revolutionary Panel-based Package RDL Configuration capable of 200-450 IO/mm/layer, an Innovation for More-Than-Moore System Integration

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Abstract

This paper presents, for the first time, a novel silicon damascene like via-in-trench (ViT) interconnect for panel-scale package redistribution layer (RDL) configuration. The panel scale damascene RDL in this paper comprises of ultra-fine copper embedded trenches and microvias with diameter equal to the width of trenches using a 5 μm thick dry film photosensitive dielectric. A 140 μm thick glass substrate is used as the core material. The new panel scalable ViT interconnect is targeted for low cost, next generation 2D and 2.5D interposers and high density packages. The ViT RDL is integrated with 2 μm diameter microvias with 2.5 μm half-line pitch copper traces embedded in a 5 μm thick dry film photo-imageable dielectric (PID) polymer. This RDL integration directly translates to IO density of 200 IO/mm/layer. IO/mm/layer, as defined by Intel, is the number of wires routed per mm of die edge on each layer of package substrate. There is no capture pad required for ViT interconnect demonstrated in this paper. The routing Cu trace is aligned directly on top of microvia instead of the conventional via-capture pad-trace interconnect configuration. The fabrication of such a high density RDL is achieved by patterning a trench over via and then fully filling with copper. Conventional i-line (365 nm) photolithography, widely used for patterning PWB and package substrates, was employed for fine trenches formation as well as small microvias in the PID. An advanced 5 μm thick PID film IF4605 was selected for build-up layers. Experimental results showed that microvias with diameters of 2 μm and trenches with half-line pitch of 2.5 μm were achieved in 5 μm thick IF dry film. Traces with half-line pitch of 1 μm were demonstrated in a 3 μm thick liquid photo resist film. The aspect ratios were 2.5 for dry film PID and 3 for liquid photo-resist respectively. The best interconnection density in terms of IO/mm/layer was calculated to be 200 using dry film PID and can be extended to 450 using thinner PIDs. For comparison, the IO density for state-of-the-art organic interposer was 40 by using semi-additive process (SAP). The embedded trench technology breaks through the limit of SAP and achieves 5-10X interconnect density compared to SAP. The ViT interconnect is a revolutionary package RDL configuration to meet the requirements of future package substrates for high performance computing, high bandwidth memory and micro-miniaturized system applications. The demonstration of ViT RDL configuration on thin glass substrate with L/S/Via/Pitch of 2.5/2.5/2/20 μm using embedded trench approach will be presented and the fabrication processes will be described in detail.

Keywords- Via-in-trench; Embedded trench, Microvia; 2.5D Interposer; SAP, Interconnect; Fly-cut; IO density

I. INTRODUCTION

The two primary considerations for 2.5D interposers and high density packages are IO density and cost. Generally, the challenge is to employ low cost package substrate fabrication technologies and increase IO density. The current semi-additive process used for high density interconnect (HDI) package substrates is facing serious challenges to scale RDL feature sizes below 6 μm . M. Ishida et.al. demonstrated traces with a minimum half-line pitch of 6 μm on organic substrate by using SAP for 2.5D organic interposer APX [1]. The IO density calculated for APX was 40 IO/mm/layer. Instead of SAP, the back-end-of-line (BEOL) RDL process is employed for wafer-scale 2.5D Si interposers for higher IO density needs. The traces with minimum half-line pitch of 0.4 μm was reported by Xilinx for VIRTEX-7 based Si-interposer [2]. The IO density for this Si interposer was 1,000 IO/mm/layer or higher. It was achieved by using 65 nm node BEOL process. It can be seen that the cost is low for organic interposer by using conventional SAP process but its IO density is very limited. On the other hand, the IO density can be very high but cost becomes a concern with the semiconductor BEOL process. There is an urgent need to develop alternative technologies to address IO density needs in the intermediate 100-500 IO/mm/layer at lower costs. The major difficulties associated with conventional SAP are seed layer etching, stability of fine traces and surface non-planarities. Embedded trench technologies have been developed to address these challenges. Figure 1 shows a schematic of the state-of-the-art package SAP RDL configuration with microvia-capture pad-trace interconnect based on organic interposer APX. The RDL via-to-via pitch is 50 μm and only one trace of 6 μm width can be escaped between two adjacent pads [1]. Figure 2 shows the schematic of the proposed new ViT RDL configuration based on photo embedded trench approach. The via-to-via pitch in this case is 20 μm and many traces can still be escaped between two adjacent pads. The major differences, as seen in Fig. 1 and Fig. 2., between the two approaches are: (1) With conventional SAP, copper traces are on the surface of the

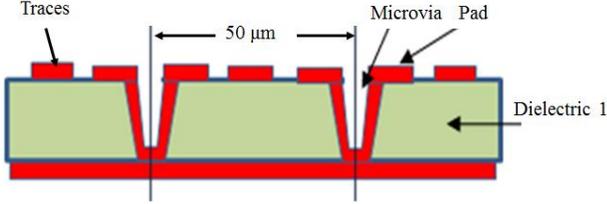


Figure 1. The scheme of state-of-the-art microvia with capture pad configuration for 2.5D Organic Interposer with 50 μm bump pitch by conventional SAP.

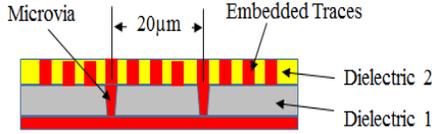


Figure 2. The schematic of novel ViT interconnect configuration for 20 μm bump pitch interposer and package application. The traces are embedded in the dielectric layer and surrounded by polymer.

dielectric layer while in ViT approach, the traces are embedded in dielectric layer and surrounded by polymer. (2) There is a need for a big pad to capture the microvia with SAP while there is no pad, but a trace directly landed on microvia with ViT. (3) Via diameter is equal to line width in ViT approach and it is much larger in the conventional SAP RDL therefore, the wiring density is much higher with ViT configuration.

Several other articles have reported the advances in embedded trench approaches [3, 4, 5]. The finest feature dimension reported so far was 1.5 μm half-line pitch by using circuit pattern transfer onto a Cu foil and photo trench approaches [5]. This paper will focus only on photo embedded trench approach. This approach addresses the key challenges of SAP.

II. CALCULATIONS OF IO DENSITY IN TERMS OF IO/MM/LAYER

The increase in bandwidth and functionality greatly drives a larger number of signal I/Os. At the same time, however, the die size is becoming smaller and smaller due to the down scaling of C-MOS semiconductor technology. Thus, the large number of IO interconnects coupled with reduction of die size pushes finer die interconnect pitches. The scaling of bump pitch to 50 μm or below is in the roadmaps of most key companies. As the bump pitch is going down, the requirement of IO density is significantly going up. IO/mm/layer, as defined by Intel for package substrate performance, is a key metric used to compare across technologies and quantify IO density [6]. IO/mm/layer is the number of wires escaping per mm of die edge for each layer of the package substrate. The theoretical best IO/mm/layer is when via diameter is the same as the trace width in the substrate. This is similar to what is achieved in a damascene process. In that case, the IO/mm/layer is just the reciprocal of the line/space pitch. The graph in Fig. 3 below illustrates the theoretical best for a given line & space.

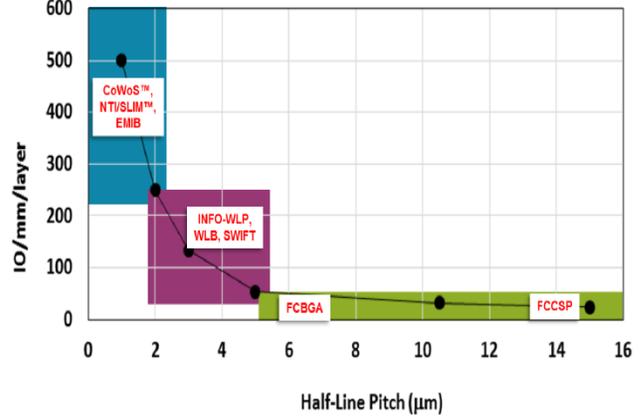


Figure 3. The IO density, IO/mm/layer, requirement for current 2D, next generation 2D and 2.5D applications (Courtesy: Intel).

In a silicon interposer, all the layers below the surface (where the micro-bumps are soldered) are damascene layers. Thus, the layers below the surface reach the theoretical maximum best IO/mm/layer. The surface layer is hindered by the micro-bump pad and has a substantially lower IO/mm. Figure 4 shows how a realistic IO/mm/layer is calculated and how the microvia and capture pad used in conventional organic interposer affects the IO density.

Assume a RDL configuration as shown in Figure 4. The routing line width and space are denoted by L and S respectively. The via diameter is d and the pitch for the vias is P. The capture pad diameter is D. The number of wires in a pitch is n. From Fig. 4, we can have

$$P = D/2 + n*(L+S) + S + D/2 \quad (1)$$

If $L=S$, the equation (1) becomes

$$P=D + (2n+1) *L \quad (2)$$

The number of escaping wires 'n' in a given pitch can be obtained by:

$$n = \{[(P-D)/L] - 1\}/2 \quad (3)$$

The IO density, IO/mm/layer, can be calculated.

$$\text{IO/mm/layer} = (n+1)/P \text{ (Unit of P is in mm)} \quad (4)$$

First, let's calculate IO density for current state-of-the-art SAP based organic interposer as shown in Fig. 1: $P = 50 \mu\text{m} = 0.050 \text{ mm}$, $d = 20 \mu\text{m}$, $D = 32 \mu\text{m}$, $L = S = 6 \mu\text{m}$, from equation (3), $n = \{[(50-32)/6] - 1\}/2 = \{3-1\}/2 = 1$. Only one wire can be escaped from a 50um pitch. From Equation (4), the IO density = $2/0.050 = 40/\text{mm/layer}$. The IO/mm/layer count for such a substrate turns out to be 40.

Next, let's calculate IO density for via-in-trench (ViT) RDL configuration shown in Fig. 2. The microvia diameter equal to or smaller than the line width and no capture pad. We have $D = d$ and $d \leq L$. Equation (3) becomes $n = [(P-L)/L - 1]/2 = (P/L - 2)/2$. The effects of via and pad are eliminated. For $P = 20 \mu\text{m} = 0.020 \text{ mm}$, $L = S = 2.5 \mu\text{m}$, the

$n = (20/2.5 - 2)/2 = 3$. The IO density in terms of IO/mm/layer = $(3+1)/0.020 = 200$. The theoretical best IO/mm/layer for this substrate is 200, which is 5X increment to that achieved by SAP with organic interposer. This demonstrates the significant improvement for RDL by using ViT embedded trench technology. When trench dimension is reduced to 1 μm , the IO density will be 450, which is 9X increment.

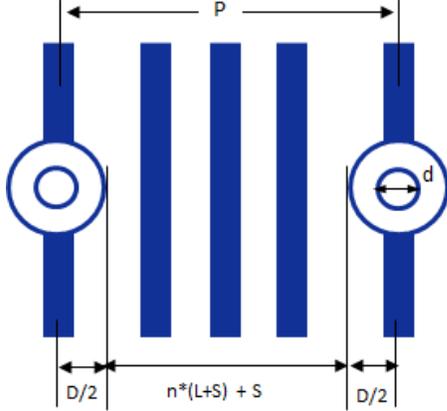


Fig. 4. Package RDL configuration and IO density calculation: L: line width, S: line space, d: via diameter, D: capture pad diameter, P: via pitch.

III. ViT APPROACH- MATERIALS AND PROCESS FLOW

A. Photo-imageable Dielectric (PID) Material

Three kinds of materials are employed in this research:

1. A thin film, high resolution, photo-imageable dielectric, IF4605 (provided by TOK), used for embedded trench and microvia layers
2. A 6" x 6" thin glass panel for substrate core or interposer core and
3. A thin ABF (Ajinomoto build-up film) for buffer layer between glass core and build-up layers.

The glass core has a flat and smooth surface necessary for fine line photolithography, high modulus and excellent dimensional stability for accurate layer-to-layer registration and low CTE of 3 ppm/K. The PID polymer IF4605 is a newly developed, advanced epoxy based chemically amplified negative tone dry film. The thickness of the film is 5 μm . It is sensitive to 365 nm (i-line) and can resolve line pitch/width of 4/2 μm with vertical walls. The film IF4605 is a key material for meeting the target high IO density requirement. Epoxy resin is the standard dielectric widely used in conventional package substrates today. Similarly, the IF film has low dielectric constant ($D_k=3.5$), low curing temperatures (200 $^{\circ}\text{C}$) and high elongation to break (20%) best suited for package applications. The chemical amplified resin uses a photo-chemically generated acid as a catalyst leading to a cascade of chemical reactions in the resin matrix that changes the solubility of the resin. The advantages of chemically amplified PID are capable for making nearly vertical wall, high aspect ratio structures independent of the minor variations in topography of the surface or film thickness. In addition, the IF film has very

low average surface roughness (R_a) of < 5 nm and low R_z (average difference of the five highest peaks and lowest valleys over the entire sampling length) of < 20 nm. This makes the film ideal for fine line lithography ($\leq 2 \mu\text{m}$). The low modulus (< 2 GPa) and high elongation to break (20 %)

Table 1. Properties of IF4605

Properties	Measurement method	IF4605
T_g ($^{\circ}\text{C}$)	DMA	250
CTE (ppm/ $^{\circ}\text{C}$)	TMA	45
Thermal weight loss temperature ($^{\circ}\text{C}$)	TG/DTA	315 (3%) 325 (5%)
Elongation to break (%)	Tensilon	20
Tensile strength (MPa)		82
Young's modulus (GPa)		1.64
Dielectric constant	CV, 1MHz	3.5
Loss Tangent	0.1 MHz	0.022

of IF4605 is useful for stress absorbance and long term reliability. In this embedded trench research, IF4605 was selected for build-up RDL dielectric layer. Both microvias and trenches were formed in IF4605 film. The minimum width of the trench in the film was 2 μm and the minimum via diameter formed was 2 μm , which is same as the trench width. The detailed process and results will be presented and discussed below. The properties of IF4605 are listed in table 1.

B. Photo Trench Formation and Metallization

The embedded trench fabrication process flow can be divided into 3 major steps: Trench formation, metallization and removal of Cu overburden from the surface.

1) Trench Formation

The first step for trench formation is lamination of a thin buffer layer on glass. A 15 μm thick ABF was used in this study as the buffer layer. IF4605 film was laminated on top of ABF and patterned by conventional 365 nm i-line photolithography. This step is similar to the normal photolithography using dry film photoresist which includes exposure and development. An additional post exposure bake step was added for the chemically amplified IF4605 film. The film was then cured at 200 $^{\circ}\text{C}$ for 1 hour.

2) Metallization of embedded trenches

Once the trenches are fabricated, the next step is of metallization to fill copper in the trenches. A thin conductive seed layer is required to provide an electrical path over the panel for electrolytic copper plating. For IF4605, physical vapor deposition (PVD) process was used

to deposit Ti/Cu seed layer. A 50 nm Ti/150 nm Cu was deposited over entire surface by sputtering. This was followed by electrolytic copper plating to plate copper over the panel. During copper plating, all the trenches are plated up. After the filling step, copper overburden is formed over the surface. The excess copper needs to be removed. In order to reduce the possible copper overburden, Via² with SuperFilling technology was developed by AtoTech [4]. In this study, a plating bath with a vertical spray nozzle system was employed for trench filling. Figure 5 shows the cross section of copper filled trenches on bare FR-4 laminate. The trench width is 5 μm and the depth is 14 μm . The overburden copper over the surface is 7 μm which is about half of the trench depth.

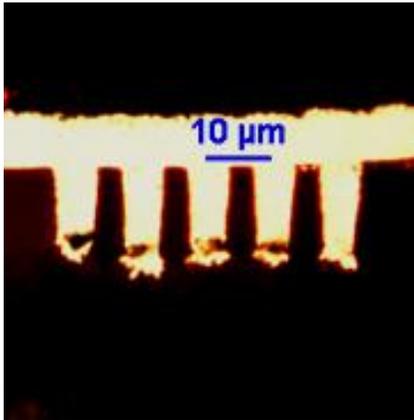


Figure 5. Cross section of copper filled trench in bare FR-4. The trench width is 5 μm and depth is 14 μm . Overburdened copper on surface is 7 μm

3) Removal of Copper Overburden

a) *Wet Etching:* Chemical wet etching was initially used to remove the overburden copper. Standard spray etchant (Copper Chloride) etches most of the copper on surface and then the micro-etching process etches the rest of thin copper and clean the residue. Figure 6 shows the cross section of embedded traces with half-line pitch of 2.5 μm after wet etching. The traces have near vertical walls and are flat on the top and bottom surfaces. There are no dimensional changes of the side walls after the etching process.

b) *Fly Cut:* Disco's Planarization tool, SURFACE PLANAR was used to remove the overburden copper. The tool works by having a single diamond bit mounted on a spindle which rotates at high RPM at a constant height. The substrate is placed on a flat chuck table and creep fed into the bit resulting in shaving of the substrate material in small amounts. Such mechanism allows the small differences in the substrate to be shaved off resulting in low overall TTV as well as removing any regional height differences. This process is preferable for ductile materials over CMP and grinding. The main advantage over CMP is the lack of slurry.

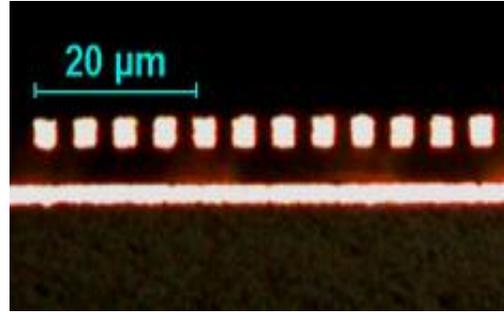


Figure 6. Half-Line Pitch of 2.5 μm trenches filled with copper in IF-4605 after chemical wet etching.

C. Microvia Formation

Both CO₂ and UV lasers are now used for microvia formation in the package substrate industry. However, both CO₂ and UV lasers have difficulties to make ultra-small vias for 2.5D interposer requirements. The via diameter limit is about 40 μm for CO₂ laser and about 20 μm for UV laser [2]. Experiments showed that ultra-small vias could be formed in IF4605 film by conventional 365 nm photolithography process. The film is cured after via formation and followed by metallization. With process optimization, 2 μm diameter vias were successfully opened and plated using a 5 μm thick IF4605 film. Figure 7 shows area array patterns of copper plated microvias with 2 μm diameter in IF4605. Since bottom up plating approach was used, the filled copper vias confirm they are opened. As seen in Figure 7, the fully filled vias have nearly perfect vertical walls.

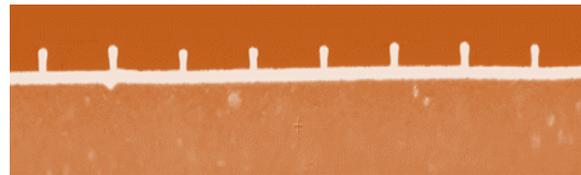


Figure 7: Microvias with 2 μm diameter formed and filled with copper using PID IF-4605

D. Integration of Embedded Trenches with Microvias

The integration process starts with via fabrication as described in section C above. After microvia processes were completed by conventional photolithography, second IF4605 film was laminated on top of via layer. Before exposing the second IF film to 365 nm UV radiation, the trench layer on the mask should be aligned with the lower microvia layer on the substrate. Donut circle marks and vernier marks were designed and plotted on the masks for this purpose. Based on these alignment marks, the registration for trenches and vias was automatically performed using Ushio's UX-44101 Projection Aligner. After UV exposure and development, the trenches were aligned directly on top of the microvias. The vernier marks were used for checking the accuracy of registration. Figure 8 shows two well aligned vernier marks after UV exposure

and development. The scale offset on the left side is $0.2\ \mu\text{m}$ and on the right is $0.4\ \mu\text{m}$.

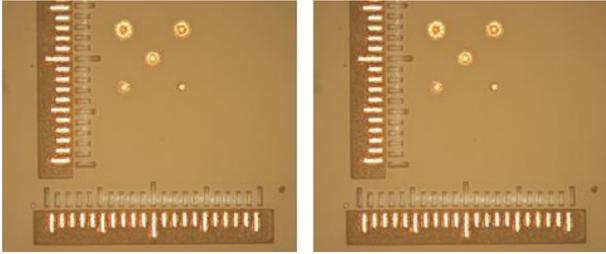


Fig. 8. Two well aligned vernier marks after fabrication with $0.2\ \mu\text{m}$ scale offset (left) and $0.4\ \mu\text{m}$ scale offset (right)

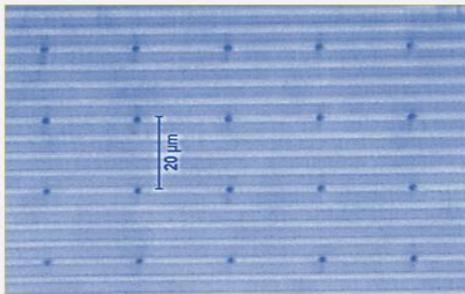


Fig. 9. Micrograph of $2.5\ \mu\text{m}$ trenches formed on top of $2\ \mu\text{m}$ microvias. The via pitch is $20\ \mu\text{m}$. Vias in trenches are clearly seen.

Figure 9 shows the top view of a test structure with area array microvias integrated with trenches. The via diameter is $2\ \mu\text{m}$ and via pitch is $20\ \mu\text{m}$. The trench width and space are $2.5\ \mu\text{m}$ each. With this feature dimensions, three trenches can be routed in a $20\ \mu\text{m}$ pitch. After the trenches are fully filled with copper and the copper overburden is removed, fully integrated structures are accomplished.

Figure 10 shows the cross section of the integrated trenches and microvias. This RDL configuration is similar to that used for semiconductor IC BEOL RDL fabricated using damascene process. This ViT structure can, therefore, be called Si-like package RDL or simply Si-like RDL. There are three trenches that can be routed in $20\ \mu\text{m}$ pitch. Total number of routing wires is four per pitch. The configuration of this new RDL is $L/S/Via/Pitch = 2.5/2.5/2/20\ \mu\text{m}$. Comparing with traditional configuration of RDL possible by SAP in Figure 1, the new generation RDL has much higher wiring density capability.

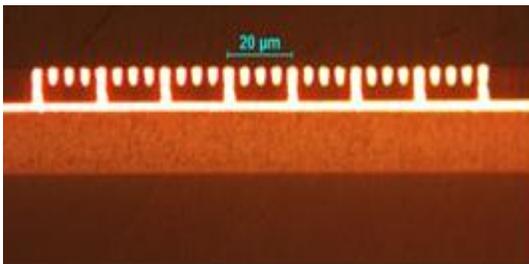


Figure 10: Cross section of Silicon-like via-in-trench (ViT) RDL on thin glass panel with $L/S/Via/Pitch$ of $2.5/2.5/2/20\ \mu\text{m}$. This RDL meets 200 IO/mm/layer requirement.

E. Embedded Trench Approach and Its Advantages

In Embedded Trench approach, the copper traces are embedded in the polymer dielectric layer and surrounded by it. There is no seed layer beneath the copper traces that needs to be etched away. Therefore, the issues related to SAP of narrowing traces after seed layer etch and fine trace adhesion stability are eliminated. Figure 11 illustrates a simplified embedded trench process flow. Figure 11(d) shows the finished RDL structure of dielectric layer and embedded copper traces with a completely planar surface.

It can be summarized that the photo embedded trench approach addresses the limitations of SAP by retaining the advantages of using photolithography to define the structure. It provides a low cost solution for next generation 2D and 2.5D interposer and package applications.

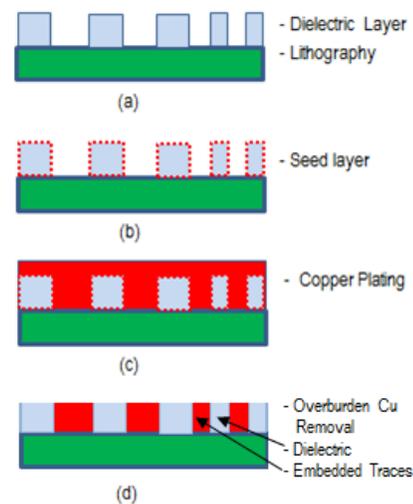


Fig. 11. Simplified Embedded Trench Process Flow (only one side shown). The traces are embedded in a dielectric layer and have a flat surface.

IV. LOW COST ONE MICRON FINE LINE LITHOGRAPHY

Photolithography is an effective and cost low method to make fine and precise patterns. It has the advantages of making the best quality geometry from sub-micron to hundred micron features. Applications like 2.5D interposers require to scale down to $1\ \mu\text{m}$ feature size at panel level for achieving IO/mm/layer close to 500. In this research, photolithography methods were studied for forming both fine pitch trenches and small microvias, thus overcoming the geometry limits and cost issues of laser ablation. With photolithography, all the structures on a mask will be transferred to substrate or interposer by one-time full field exposure. Laser ablation can also be used to make circuitry patterns. However, today with laser ablation, the feature sizes around a certain range, $10\text{-}30\ \mu\text{m}$, are cost effective. Large size features require ablating large amount of materials which takes more time and more energy leading to high cost. Small size features require small laser beam which requires high quality optics to focus the beam and precise mechanical systems to control beam movement. The minimum trench demonstrated by excimer laser ablation was $5\text{-}7\ \mu\text{m}$ [7].

There are three basic photolithographic models used in high density PCB and package substrates: proximity, contact and projection. Proximity and contact models are being widely used for feature sizes larger than 10 μm using dry film photo resists due to its low cost. When feature sizes scale below 10 μm, projection lithography tool is being used. The best resolution projection lithography based stepper tools used in package substrates today is 2 μm, such as Ushio Aligner UX-44101 and Rudolph JetStep series. Higher resolution projection steppers used in semiconductor IC fabrication with large NA optical imaging systems and short wavelengths are complex, have short depth of focus and expensive.

A. Projection Mask Aligner:

An advanced projection stepper tool, UX-44101 from Ushio, was used for fine line photolithography. This tool is equipped with a high power i-line (λ = 365nm) light source and has 2 μm resolution in a 100 mm round or 70 mm x 70 mm large-panel exposure area with ±1 μm alignment accuracy. The tool has +/- 10 μm depth of focus (DOF) to accommodate thick photoresists for high aspect ratio structures, substrate warpage and non-planar surface. The resolution for a projection mask aligner is

$$R = K_1\lambda/NA \tag{5}$$

K₁: a constant factor affected by material and process used, generally lies in the range of 0.5-1 for 365 nm lithography. It can be determined by experiments.

NA: Optical numerical aperture, lower NA is mostly likely to be used for litho tools in package substrate industry.

Assuming NA = 0.15, K = 0.5-1, for i-line λ = 365 nm, R = K₁*0.365/0.15 = 2.4*K₁ = 1.2-2.4 μm. Increase of NA will result in higher resolution. However, the depth-of-focus (DOF) will become narrower.

The DOF for a projection mask aligner is

$$DOF = K_2\lambda/(NA)^2 \tag{6}$$

K₂ is similar to K₁, If NA increased to 2 times large, resolution does become half. But, the DOF will be reduced from 10 μm to 2.5 μm, which is too small for package substrate applications.

Figure 12 shows traces with half-line pitch of 2 to 5 μm formed in IF4605 film by using UX-44101 projection stepper.

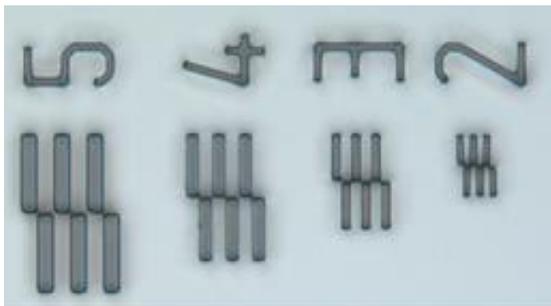


Fig. 12. Test structure of half-line pitch of 2 to 5 μm in IF4605 PID by using UX-44101 projection stepper. Aspect ratios of upto 2.5 can be patterned in IF4605 using UX-44101.

B. Contact Mask Aligner:

In general, a minimum feature size of 3 to 4 μm could be achieved at the gap of 10 μm using proximity photolithography model. For the requirement of 1 to 2 μm critical dimension, the proximity mode would be forced to go into contact mode. Two contact mask aligners were used in this study: an old generation Tamarack (over 35 years old) and Karl Suss MA-6 Mask Aligner. Both the contact mask aligners operate at 365 nm wavelength (i-line). Simulations based on near field Fresnel diffraction show that, when the gap is at 1 μm or less, traces with half-line pitch of 1 μm can be resolved. Simulation results are shown in Figure 13. Comb structures with half-line pitch of 1 μm were achieved using both tools. Figures 14 (a) and 14 (b) show feature sizes of 1/1 μm and 1.5/1.5 μm using 3 μm thick liquid spun-on photo resist.

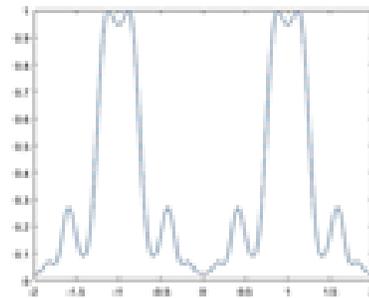


Fig. 13. Simulation of light intensity distribution with gap of 1 μm through a comb structure with pitch/width of 2/1 μm.

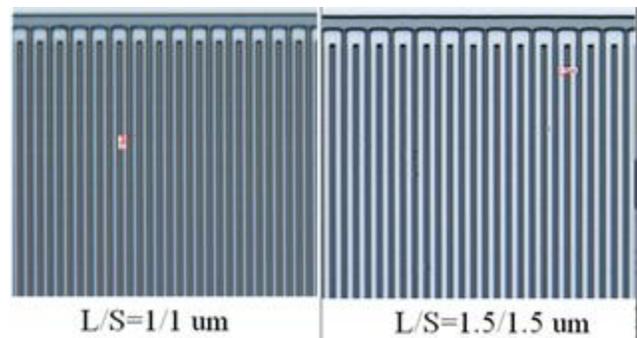


Fig. 14 (a). Traces patterned using 3 μm thick SC1800 photo resist with i-line contact photolithography. The half-line pitch of traces are 1 μm (left) and 1.5 μm (right).

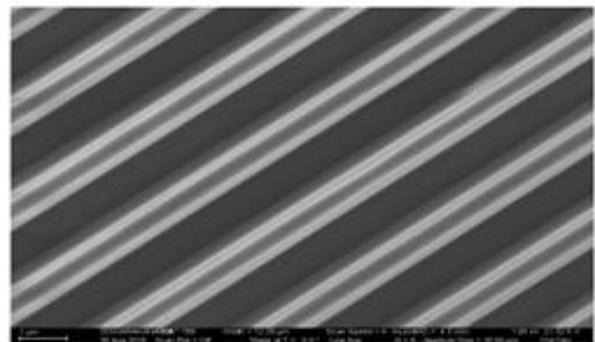


Figure 14 (b). SEM image of SC photo resist features of half-line pitch of 1 μm formed with i-line contact photolithography

V. SUMMARY

The RDL IO density is the most critical parameter for 2.5D interposers and other high performance applications for system-scale integration and miniaturization. The requirements and challenges based on current packaging substrate technologies were discussed. The advantages and limitations of semi-additive and embedded trench processes were analyzed and compared. The latter approach breaks through the limits of SAP by retaining the advantages of SAP while overcoming its challenges. A novel via-in-trench (ViT) package RDL configuration based on embedded trench approach was proposed and a Si-like RDL with L/S/Via/Pitch of 2.5/2.5/2/20 μm was demonstrated. This high density RDL matches the IO density of 200 IO/mm/layer, 5X higher than the current SAP technology. It is possible to extend IO density further to 450 with novel photolithography approaches. The new ViT interconnect technology can be applied to mobile fan-out technologies like INFO-WLP, SWIFT, high-end server interposer packages like CoWoS, NTI/SLIM, EMIB. The via-in-trench interconnect can be considered as a revolutionary package RDL configuration for next generation 2D, 2.5D and 3D interposers and packages. It is crucial to the success of more-than-Moore system integration.

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VII. REFERENCES

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