First Demonstration of Panel Glass Fan-out (GFO) Packages for High I/O Density and High Frequency Multi-Chip Integration

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Abstract— Ultra-thin, panel-level glass fan-out packages (GFO) were demonstrated for next-generation fan-out packaging with high-density high-performance digital, analog, power, RF and mm-wave applications. The key advances with GFO include: 1) large area panel-scalable glass substrate processes with lower cost, 2) silicon-like RDL on large panels with 1-2 µm critical dimensions (CD), 3) lower interconnect loss and 4) improved board-level reliability enabled by the tailorability of the CTE of the glass panels and compliant interconnections. Daisy-chain test dies were used to emulate an embedded device with the size of 6.469 mm x 5.902 mm, thickness of 75 µm and pad pitch of 65 µm. Glass panels with 70 µm thickness and through-glass cavities were first fabricated, and then bonded onto a 50 µm thick glass panel carrier using adhesives. After glass-to-glass bonding, the test dies were assembled into the glass cavities using a high-speed placement tool. RDL polymers were then laminated onto both sides and cured to minimize the warpage of the ultra-thin package. A surface planar tool was then used to planarize the surface of the panel to expose the copper microbumps on the die, followed by a standard semi-additive process (SAP) for the fan-out RDL layer. The shift and warpage of the die were characterized during the multiple process steps. Initial modeling and measured results indicate the potential for less than 5 µm die shift and less than 10-15 µm warpage across a 300 mm x 300 mm panel size.

Keywords – ultra-thin; Glass Fan-out (GFO) Package; panel-level; high I/O density; die-shift; warpage.

I. INTRODUCTION

Fan-out wafer level packages (FO-WLP) are poised to disrupt the entire semiconductor industry due to their size, cost, performance and reliability benefits compared to traditional flip-chip and wire bond packages. Although they were initially designed to extend package I/O counts beyond fan-in Wafer Level Packages (WLP), the scope of FO-WLP technology has expanded significantly in recent years to include multi-component SiP modules, as well as high I/O logic and memory integration. The driving factors for the implementation of FO-WLP technology are the associated low packaging and test costs, excellent electrical and thermal performance, improved reliability compared to WLP, and the potential for heterogeneous integration.

One example of packaging for high chip-level I/O density applications is TSMC's integrated fan-out (InFO) [1] for Apple iPhone 7 in 2016, as shown in Figure 1.

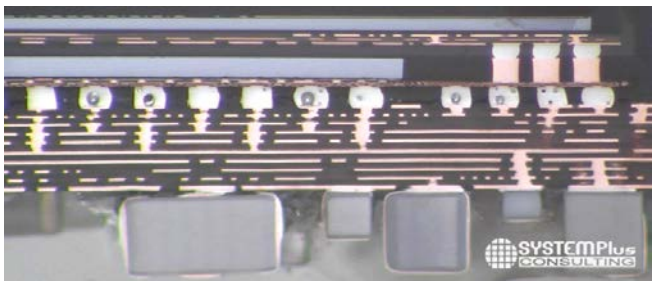


Figure 1. TSMC's InFO package for processor-memory stacking (System Plus and Yole).

A major concern of FO-WLP with chip-first embedding of high value-add and high I/O CPUs and GPUs is the yield loss of ICs during RDL fabrication. The same concern applies to high-value multi-chip modules that can't be thrown away, if not yielded. Amkor addressed this concern by developing Silicon Wafer Integrated Fan-out Technology (SWIFT) [2], a chip-last approach as shown in Figure 2. This method was demonstrated with RDL lines as low as 2µm.

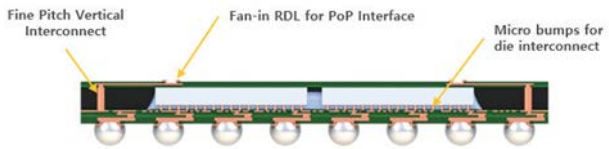


Figure 2. Silicon Wafer Integrated Fan-out Technology (SWIFT) by Amkor.

A major trend in fan-out packaging is the move to large panel formats, so-called panel level packaging (FO-PLP) to increase productivity and further reduce cost. The economies of scale of panel-based processing may reduce FO-WLP cost from 20-40%, up to 2-4X, depending on the package and panel sizes, and the number of die per package. FO-PLP technologies can be broadly classified into 1) laminate embedded solutions, such as Imbera's Integrated Module Board (IMB) [3], AT&S's Embedded Components Packaging (ECP) [4], and ASE's advanced – Embedded Assembly Solution Integration (a-EASI) [5]; 2) panel fan-

out solutions, including Amkor/J-Devices Wide Strip Panel Fan-out Package (WFOP) [6], PTI's panel-scale molded fan-out, and 3) chip-last PLP, such as ASE's coreless embedded trace approach. Panel sizes up to 24'' x 18''/610 mm x 457 mm have been demonstrated by applying current laminate or PWB infrastructure, or new hybrid process lines [7, 8]. However, there is a continuing need to improve I/O density, high-frequency performance, yield & cost and board-level reliability beyond current FO-WLP and FO-PLP approaches. This need can be comprehensively addressed by using glass as the fan-out substrate. A schematic of the glass fan-out package is shown in Figure 3.

A panel-level Glass Fan-out packaging approach was demonstrated for higher I/O and component density, lower interconnect loss, and higher board-level reliability. The silicon-like dimensional stability of glass in large panel manufacturing will bring an unparalleled combination of high I/Os and low cost not possible in laminate or mold compound based fan-out. The low-loss tangent of glass by a factor of ~2-3x compared to mold compound [9,10], makes GFO an ideal candidate for RF and mm-wave modules. Unlike high-density fan-out packages that require an organic package to connect to boards for large body sizes, GFO packages are designed to be directly-SMT attached to the board, enabled by the tailorability of the CTE of the glass panels and compliant interconnections. Lastly, the ultra-smooth surface and high dimensional stability of glass enables silicon-like RDL capability on large panels for the first time, with 1-2µm critical dimensions (CD) for high density fan-out applications.

GFO, however, needs to address process challenges associated with glass-handling, cavity-formation with precision, and planarization of embedded-die packages. By developing unique process advances to address these challenges, ultra-thin, panel-level glass fan-out packages (GFO) for higher I/O and component density, lower interconnect loss, and higher board-level reliability were demonstrated for the first time.

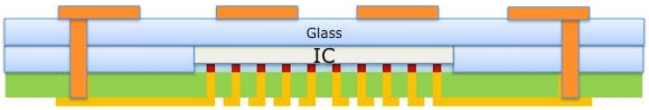


Figure 3. Schematic cross-section illustrating Georgia Tech's GFO approach.

II. Demonstration of GFO Package

The process flow for GFO package fabrication is shown in Figure 4. Glass panels with 70 µm thickness and through-glass cavities were first fabricated with precise cavity location and dimension accuracy below +5 µm, and then then bonded onto a 50 µm thick glass panel carrier using adhesives, but not cured to retain tackiness for subsequent die-assembly process. After glass-to-glass bonding, the test dies were assembled into the glass cavities using a high-speed placement tool (Kulicke and Soffa). RDL polymers were then laminated onto both sides, and simultaneosuly cured to minimize the warpage of the ultra-thin package. A surface planarization tool by Disco was then used to planarize the surface of the panel and expose the copper microbumps on the die. Fan-out redistribution traces were formed following a standard semi-additive process (SAP).

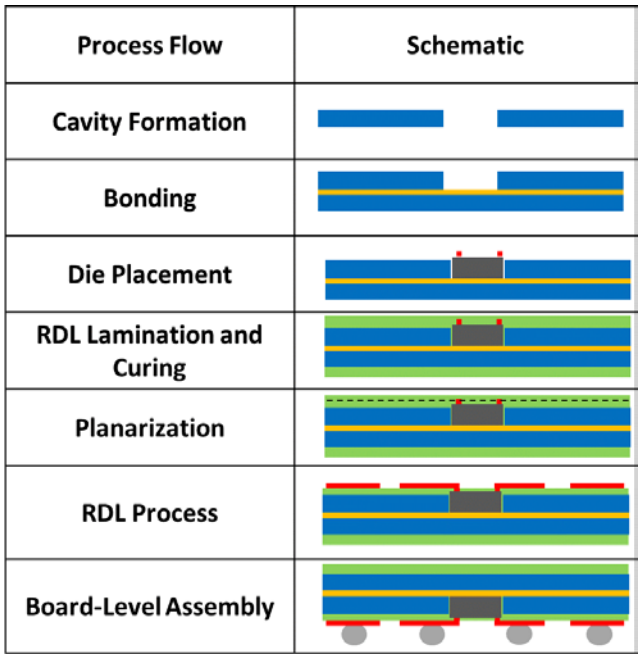


Figure 4. Process flow for GFO.

A. Glass Cavity Formation and Bonding

Precise cavity formation in glass can be realized by various methods, including laser ablation, wet etching, mechanical dicing, sand blasting, ultrasound machine or the use of photo-sensitive glass, as shown in Figure 5.

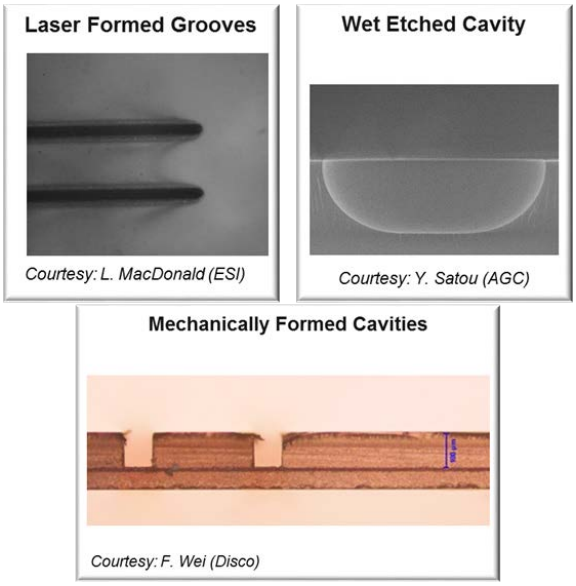
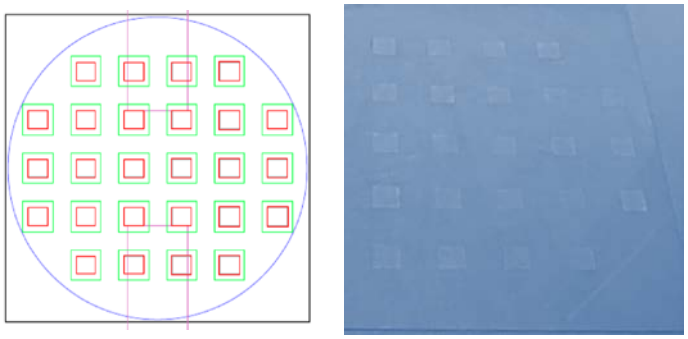


Figure 5. Glass-cavity cross-section from various fabrication methods.

The first step in GFO technology is designing through-glass cavities. Figure 6 (a) shows the design of glass panels with thickness of 70 µm, size of 300 mm x 300 mm and 26 through glass cavities in each panel. The cavities were formed using a combination of laser ablation and mechanical dicing. The top view of the fabricated glass cavity panel is shown in Figure 6 (b), with cavity location and dimension accuracy below +5 µm.



(a) (b)

Figure 6. Top view of glass cavity panel (a) designed, (b) fabricated.

The glass-cavity layer was then bonded to a 50 µm thick glass panel carrier with dry film adhesive. In order to study the adhesive strength of different glass-to-glass bonding adhesives, a 150 µm thick glass chip with the size of a quarter inch by a half inch was bonded to a glass carrier first, and then the maximum shearing pressure was tested, as shown in Figure 7. The maximum shearing pressure of different glass-to-glass bonding materials are compiled in Table 1. Based on the results, BCB dry films showed the best adhesion performance among all the tested materials.

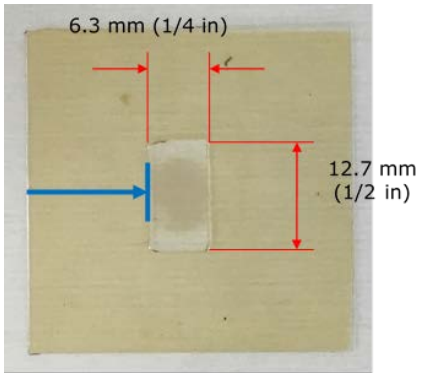


Figure 7. Test-structures to characterize glass-to-glass bonding.

TABLE I. MAXIMUM GLASS-TO-GLASS SHEAR STRENGTH OF WITH DIFFERENT ADHESIVES.

Material	**Thickness (µm)**	**Max. Shearing Pressure (MPa)**
BCB dry film	10	15.27
BCB 4026-46 liquid	9-11	2.83
film		
ABF GX-92	15	6.56
ABF GY-11	15	2.4
EPR liquid film	10	7.24

B. Die Placement

Daisy-chain test dies provided by Intel were used to emulate the embedded devices. The key characteristics of the die are: size - 6.469 mm x 5.902 mm, thickness - 75 µm, pad pitch 65 µm, and Cu bump thickness - 20 µm. The top right corner of Intel test die is shown in Figure 8.

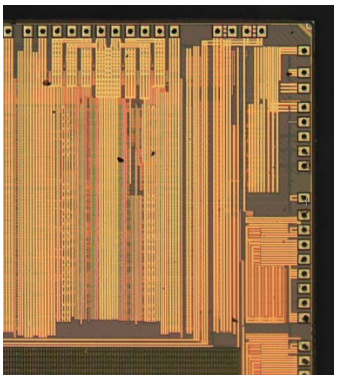


Figure 8. Optical image of the top right corner of Intel Test Chip

The effect of different die placement conditions such as temperature, tool size and force was investigated. Test chips were first assembled onto a 50 µm thick glass panel carrier with a dryfilm adhesive layer using a high-speed placement tool from Kulicke and Soffa, as shown in Figure 9.

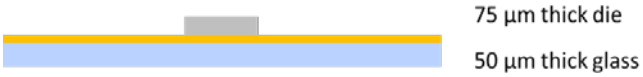
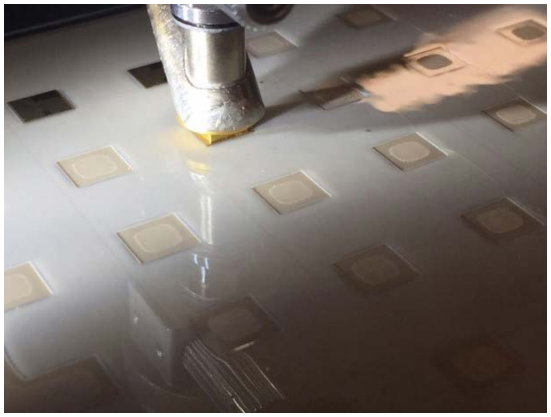
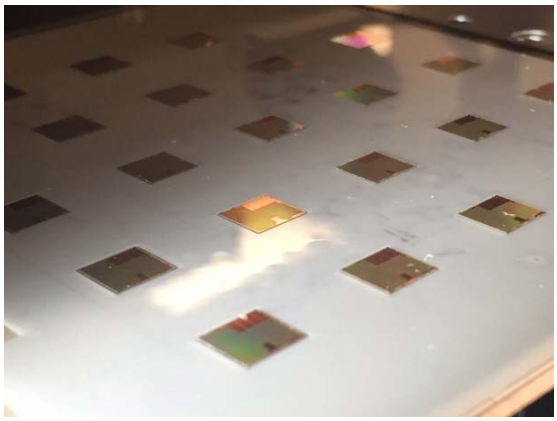


Figure 9. Test-structure for optimizing the die assembly process.

The optimized die-placement conditions such as bonding force, temperature and cycle time were determined and then applied to the assembly process in the glass cavities. Figure 10 a) shows the die placement process and Figure 10 b) shows the dies embedded in glass cavities after die placement.



(a)



(b)

Figure 10. (a) Die placement in glass cavities; (b) Optical image of embedded dies in the cavities.

C. RDL Lamination and Curing

After the dies were placed in glass cavities, RDL polymers were then laminated onto both sides and cured to minimize the warpage of the ultra-thin package. Figure 11 shows the top view of the GFO package after polymer lamination.

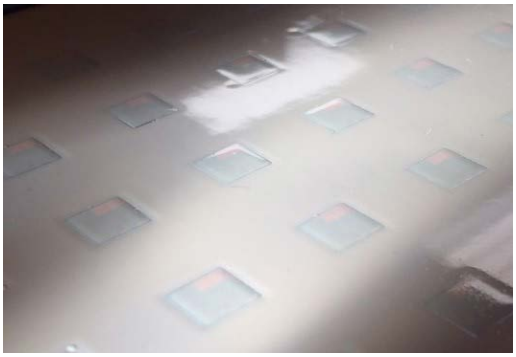


Figure 11. Top view of GFO package after polymer lamination

D. Planarization

After polymer lamination and curing, a surface planaraziation tool by Disco was then used to planarize the surface of the panel and expose the copper microbumps on the die. A smooth surface of the Cu bump was observed after planarization, as shown in Figure 12.

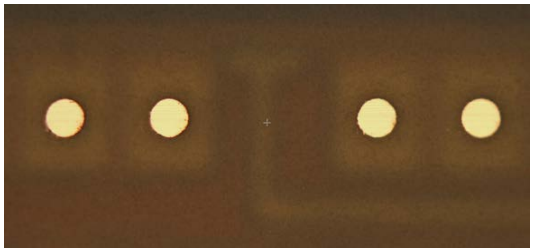


Figure 12. Top view of GFO package after planarization

E. RDL Process

Following the planarization process, a standard semi-additive process (SAP) was applied for patterning the Cu trace connected to the planarized Cu bump. The cross-section of the GFO package is shown in Figure 13. The total thickness of the GFO package is 213.8 µm, including a 50 µm thick glass carrier, a 70 µm thick glass cavity panel, 75 µm thick test chips embedded in the glass cavity, the bonding dry film and the double-side RDL polymers.

Compared to other fan-out packages, GFO packages are ultra-thin, with thickness less than 215 µm without the need for grinding. Furthermore, unlike high-density fan-out packages that require an organic package to connect to boards for large body sizes, GFO packages are designed to be directly-SMT attached to the board, enabled by the tailorability of the CTE of the glass panels and compliant interconnections. Lastly, the ultra-smooth surface and high dimensional stability of glass enables silicon-like RDL capability on large panels, with the potential of 1-2µm critical dimensions (CD) for high density fan-out applications.

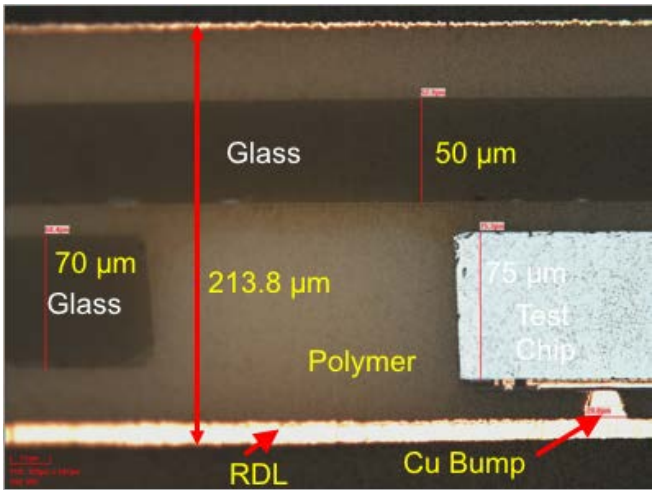
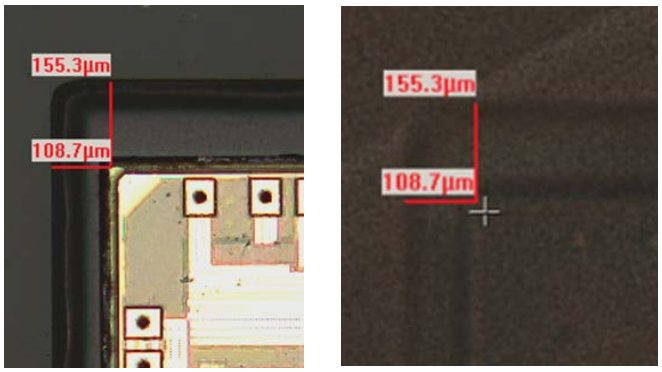


Figure 13. Cross-section of an ultra-thin Glass fan-out (GFO) package for high I/O applications.

III. Characterization of GFO Packages

A. *Die Shift*

The x, y distances between the die corner and the glass cavity corner were measured before and after polymer lamination and curing. The die-shift comparisons are shown in Figure 14. Less than 5 µm die-shifts were observed among all the 52 dies that were characterized.



(a) (b)

Figure 14. Top view of top left corner (a) after die placement, and (b) after polymer lamination and curing.

B. *Warpage*

Warpage of the dies at different locations of the whole panel was measured after die placement. The temperature was set to increase from 30 °C to 100 °C. Figure 15 shows the plot of warpage measurements along the die for five dies that are distributed at the center and four corners of the panel. It can be observed that the warpage remains below 15 µm as the temperature increases, and the temperature does not have a strong effect on the warpage.

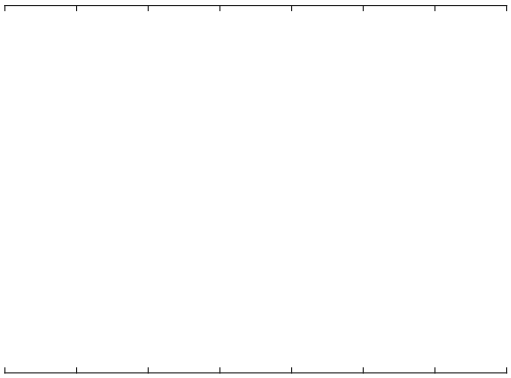


Figure 15. Warpage measurement across the die for 5 different assemblies at different locations on the panel.

IV. Conclusions

Ultra-thin, panel-level glass fan-out packages (GFO) were demonstrated with unique set of process advances. Precise cavities were formed in glass panels with low-cost and scalable processes. Cavity die-assembly processes were developed and optimized. The GFO structure provides design freedom to minimize warpage. Innovative surface planarization techniques were used to eliminate the need for blind via formation onto the die pads. Initial modeling and measured results indicate the potential for less than 5 µm die shift and less than 10-15 µm warpage across a 300mm x 300mm panel size. This unique technology has the potential to serve the next-generation fan-out packaging needs for higher I/O and component density, lower interconnect loss, and higher board-level reliability.

Acknowledgments

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