Integrated Copper Heat Slugs and EMI Shields in Panel Laminate (LFO) and Glass Fanout (GFO) Packages for High Power RF ICs

Venky Sundaram, Bartlet Deprospo, Nahid Gezgin, Atomu Watanabe, P. Markondeya Raj, Fuhan Liu, Waylon Puckett, Samuel Graham, Rao Tummala
Kyle Byers*, Sean Garrison*, Garth Kraus[#], Michael Elsbury[#]
3D Systems Packaging Research Center, Georgia Institute of Technology,
813 Ferst Dr N.W., Atlanta, GA 30332.
[#]Sandia National Labs, Albuquerque, NM
*Kansas City National Security Campus, Kansas City, MO
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Email: vs24@gatech.edu

Abstract

This paper demonstrates for the first time, ultra-thin, panel laminate fan-out (LFO) and glass fan-out (GFO) packages with embedded copper heat spreaders and electromagnetic shields for packaging high power RF ICs in much smaller form factors and at potentially much lower cost than current ceramic and metal flange packages. This unique double sided package addresses the thermal dissipation requirements of 30-100W power amplifiers by bonding the IC directly to a large copper heat spreader embedded in the substrate, using high thermal conductivity die attach paste. It also addresses the RF, microwave and mm-wave performance requirements by utilizing low loss tangent glass and polymer dielectrics, as opposed to lossy epoxy dielectrics or mold compounds. The combination of glass and high temperature polymers also enables superior harsh environment reliability with built-in stress buffer layers to mitigate the CTE mismatch induced stresses from large copper thermal structures.

1. Introduction

High peak power and high efficiency RF and mm-wave ICs such as GaN and GaAs have been widely deployed in defense applications for decades and are now gaining prominence in commercial applications such as 5G base stations and IoT networks. Such devices require very high power efficiency and ultra-low loss packages that must also deal with the extremely high, localized heat generated by the amplifiers. These high power RF ICs have been traditionally packaged in bulky ceramic and metal packages, with outstanding reliability. The ceramic packages, however, suffer from miniaturization limits as well as high cost coming from small panel sizes used for fabrication and assembly. Although a number of wafer level fanout packages (FO-WLP) have been developed in high volume manufacturing recently, the use of hygroscopic and low temperature epoxy molding compounds has limited the use of QFN and lead frame packages to lower power levels typical of low noise amplifiers. Hence, there is a critical need for new package materials and processes that can effectively meet the electrical, thermal and thermo-mechanical requirements of future high power RF IC modules for high volume applications.

Packaging design decisions are tied to many different variables including the types of components, power levels and density, form factor, and expected environments. This research is focused on radio frequency (RF) designs that require packaging of multiple radio frequency integrated circuits (RFICs) that generate head and require high isolation from one die to the next.

Previous studies have investigated low temperature co-fired ceramic (LTCC) and thin film deposition for its attractiveness in terms of reliability, durability, conductivity, good line tolerance, good line edge tolerance, wire bond connectivity, solder connectivity, miniaturization, reworkability and aging performance [1]. Several challenges exist for LTCC processing such as co-fired panel size variation, defects due to improper alignment, and shrinkage tolerance, which can be improved through processing steps and circuit design [2-4]. Similar design features listed above are still relevant, but industry trends over the past decade and packaging innovations motivate the authors to more thoroughly investigate laminate and emerging glass substrates.

In contrast to current molded or ceramic packages, this work demonstrates panel-level laminate fan-out (LFO) and Glass Fan-out (GFO) packages for lowest interconnect loss, and integrates for the first time, large copper thermal structures in thin glass substrates for improved heat dissipation. A schematic of the package structure for LFO and GFO packages with embedded heat spreaders and EMI shield walls is shown in Figure 1.

Figure 1. Laminate (LFO) or Glass Fanout (GFO) with Integrated Heat Spreaders and EMI Shields

In addition to the cost and productivity benefits of scaling to large panel sizes, there are three major performance benefits of such a package structure for high power RF ICs, (a) Ultra-short and all copper interconnections from IC to package for ultra-low inductance and signal loss at GHz frequencies, (b) large copper integrated directly under the ICs to remove heat effectively and maintain low junction temperatures in the presence of hot spots, and (c) embedded copper trench structures integrated into the same substrate as well to provide high degree of isolation between multiple RF ICs embedded in the package.

The LFO and GFO packages demonstrated in this paper lead to significant reduction in X, Y and Z form factor of high power RF IC multi-die packages, but lead to a number of fundamental challenges. The first challenge is the higher power and thermal density in the package, since embedded power amplifiers can create hot spots inside the substrate, leading to thermally induced failures if the heat is not removed at a high rate of flux. Glass is an excellent high-temperature substrate material, but its poor thermal conductivity poses thermal challenges for high power ICs. Cooling is accomplished with large copper through-via structures, copper slugs or heat spreaders, thus eliminating the hotspots and reliability issues with embedded high-power dies. The integration of large amount of copper in glass packages causes large thermo-mechanical stresses from CTE mismatch between copper and glass. Modeling and design of copper heat spreader structures with buffer layers is critical to minimize the stress in glass. Thick copper structures (>60 microns) show higher probability of glass cracking at the corners. Polymer liners act as a stress-buffer, and finite element modeling with various geometric parameters was used to arrive at the appropriate design parameters.

The final challenge of embedding multiple RF ICs in close proximity is the need for effective EMI Shielding to isolate the transmit and receive chains from each other to allow Tx and Rx channels to operate simultaneously. The shield structures should also be designed such that they don't interfere with the performance of the individual components.

This paper is organized as follows. Section 2 describes the basic research in design for EMI shielding of multiple RF ICs. Section 3 discusses the thermal modeling to design the appropriate copper heat spreader structures in the fanout packages. Section 4 describes the initial process flow used to fabricate the packages and preliminary demonstration of the LFO package with integrated heat spreaders. The last section summarizes the key findings from this research.

2a. EMI Shielding

Electromagnetic coupling or cross-talk results in performance degradation and electromagnetic compatibility issues. With increased multi-functional integration and miniaturization of emerging consumer, IoT, and automotive electronics, package and component-level EMI shielding has become extremely important to prevent undesired electromagnetic (EM) coupling.

EMI noise in traditional modules with large components is shielded by metallic cans or creating physical separation between them. Shielding with conformal metal coatings on overmolded packages has also been demonstrated. Component-level shielding has been developed with integrated via- or trench-based shields inside packages. Extensive studies have been conducted on the performance of metal-filled vias in isolating striplines and microstrip lines [5]. It was observed that a continuous fence of vias was better than intermittent fence of vias since the latter increased the radiation loss and reflections by perturbing the propagating mode. Additionally, a distance of three times the substrate height was deduced to be the optimal spacing between a via fence and a transmission line. The vias were recommended to be drilled with the least possible spacing between each other. Further, via fences were found to be effective only if the via pads were shorted both on the top and the bottom.

EMI in embedded-die RF packages was analyzed to provide initial design guidelines to achieve isolation of more than 70 dB in the frequency range of 100kHz to 3GHz. Since undesired EM coupling occurs both from above and below the substrates, innovative trench shielding structures with through-substrate vias or micro-vias are designed to achieve shielding from 2-4 GHz with component separation of below 0.5 mm.

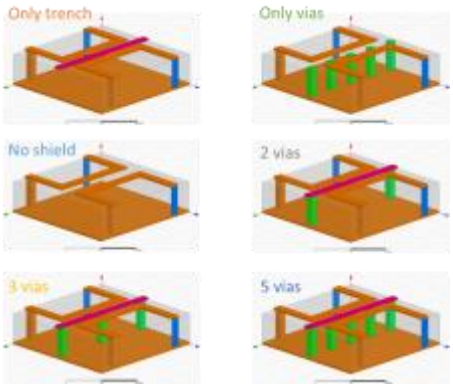
2b. EMI simulations

The type of structures that are employed for shielding is an important consideration in shield design. It is also important that the structure is compatible with the fabrication process for easy integration with the rest of the sub-system. Copper is used as the shield material because of its excellent conductivity and fabrication with standard plating processes. Two types of structures were identified – vias and trenches. The shielding effectiveness of via array is compared with that of trenches, in a multi-layer package substrate through full-wave EM simulations. Test structures comprising of microstrop transmission lines were modeled to analyze the effectiveness of various shield structures. Far-end crosstalk is an important parameter that represents the shielding between these lines. It was used to study the shield effectiveness of the structure in between. The set-up is depicted in Figure 1, where each transmission line is terminated with 50-ohms on one end and probed at the other.

In order to study the coupling between package elements, simulations were performed using HFSS – a full-wave 3D EM tool. The geometries of the transmission lines and shielding elements were selected based on the design rules. Microstrip type transmission lines with width of 40 µm and length 40 mm were used. The transmission lines were not impedance-matched to 50Ω to facilitate larger radiation. This, in turn, depicts the worst-case EM interference scenario. The TPV to the ground plane has a diameter was 60µm. In order to analyze the coupling between these elements, two of these elements were integrated into a 3D EM model, assuming 400µm of separation between the elements. The simulation was performed from 100MHz to 5 GHz, in steps of 100MHz. The top view of the typical simulation set-up consisting of a TPV, a capacitor, an inductor and a transmission line (TL) is shown in Figure 1.

2c. Trench shields grounded with via-array

Simple via-array shields with isolated pads do not reduce the coupling between the transmission lines. This is shown in Figure 2. Alternatively, when the pads are connected as trench, the reduction in coupling due to via-array shield is the same as that due to a trench-based shield. When a continuous trench that is grounded with a set of vias is used, the shielding effectiveness matched that of grounded trench-based shields. The 3D view of the via-array shields in this configuration is shown in Figure 1. The simulation results of these cases are compared with that of continuous trench in Figure 2. This is explained in Figure 3.



(a) (b)

Figure 1. Simulation setup of the via-array shields, with (a) continuous via pad, (b) discrete via pads.

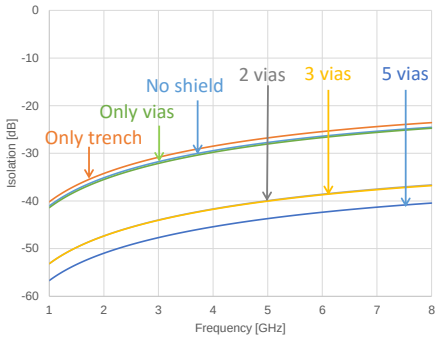


Figure 2. Comparison of TL-TL coupling in presence of trenches and different via-arrays configurations.

Since the lowest frequency of propagation depends on the largest aperture, the small aperture in the via-array with the continuous pad prevents the frequencies in 1-20 GHz from propagating through the shield; whereas, in case of the via-array with discrete pads, the unbounded aperture allows all frequencies to pass through.

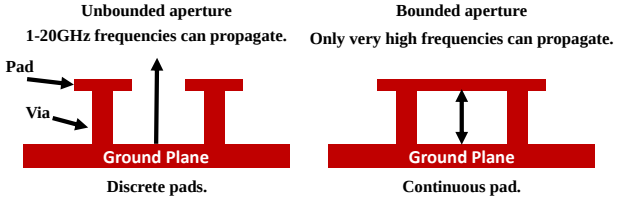


Figure 3. Lateral view of via-array shields to compare the aperture for different scenarios.

2d. Extended trench-based shields

The coupling between two microstrip transmission lines was also simulated with the trench-based shield extended vertically upwards such that it was taller than the transmission lines. The height of the trench above the transmission line was set at 20µm and 40µm, and the couplings between the transmission lines were studied. Since microstrip transmission lines are referenced to a ground plane only on the bottom, they radiate more above the plane containing the signal lines. The presence of a trench shield above the plane of the transmission line was found to improve the shielding between the transmission lines. The 3D view of the trench-based shield extending above the plane of the signal lines is shown in Figure 4. The couplings between the transmission lines for both vertical heights were compared through simulations and are shown in Figure 5. It can be seen from Figure 5 that, as the height of the trench above the transmission line increases by 20µm, the coupling reduces by 3dB. Typical tradeoff while employing such trenches would involve a compromise between the shield effectiveness and the maximum thickness of trench that can be fabricated above the plane of a transmission line.

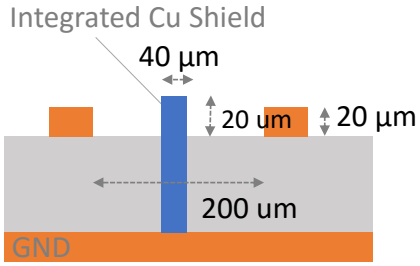


Figure 4. 3D view of the trench-based shield extending above the plane of the signal lines.

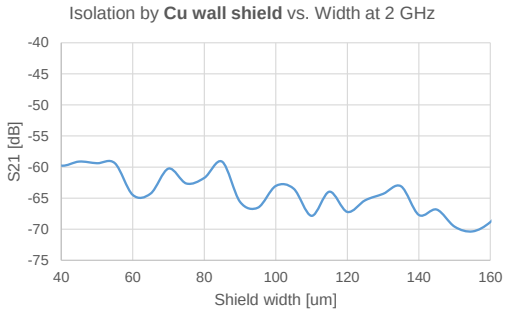


Figure 5. Comparison of TL-TL coupling for different trench configurations.

Simulation results suggest that shields consisting of only trench or only vias do not provide high shielding effectiveness. Moreover, integrating multiple vias showed the highest shielding effectiveness than the shields with a trench and two vias or three vias. The shield effectiveness with this shield design approaches that of copper wall shields. However, wall shields with width of above 100 microns showed EMI isolation of 70 dB.

2e. EMI Shielding Summary

In order to integrate shielding materials into embedded die RF packages, integrated Cu trench test structures were modeled and designed. Component-level isolation of above 60dB is achieved in the frequency range of 1- 20GHz, between transmission lines separated by less than 500µm. Trench-based shields having a width of 45µm were modeled, designed, fabricated and characterized to provide up to 20 dB of additional shielding between a pair of transmission lines, compared to via-array shields. Integration of these shield structures do not contribute significantly to the size of the module. These trench-via array structures are now being extended to 5G and other mm-wave modules in the frequency range of 28 GHz to 39 GHz.

3. Thermal Modeling of High Power RF IC Glass Fan-out Packages

In order to characterize the thermal performance of the GFO RF package, and determine the effect of changing the thickness of the Cu heat paddle, the system was numerically modeled with the steady state thermal package of ANSYS. The TGA2814 GaN RF amplifier from TriQuint, [6], was chosen to model the chip layout from. The RF chip was modeled as a 6.5 x 5.9 x 0.75 mm piece of SiC with a 2 µm layer of GaN on top. Between the GaN device, and the SiC substrate is a buffer layer which is required to grow high quality GaN, [7], however this buffer layer also severs as a large thermal boundary resistance (TBR). This TBR limits high power operation of GaN devices at by creating a large temperature difference across the buffer layer, making this an important aspect to properly model. Since this TBR layer is very thin, a few nanometers, relative to the SiC and GaN layers, tens of microns, it was modeled as an interface conductance of 4.2 K-m^2/GW with no thickness, [8]. The RF test chip was attached to a 6 x 6 mm copper heat paddle by Au-Sn solder, and the heat paddle was attached to an aluminum heat sink with the same solder, which was modeled with interface conductance of 0.877 K-m^2/MW. The test chip and heat paddle were surrounded by the glass fan-out so the outside package dimensions were 10 x 10 mm, as shown in fig 6.

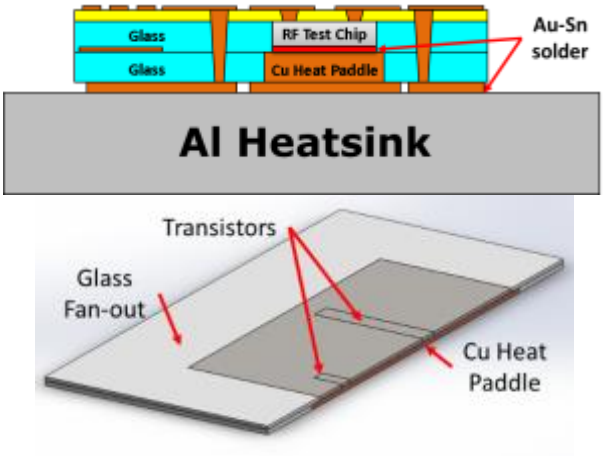


Fig 6. Thermal stack and test package used to model thermal performance.

The aluminum heat sink was modeled as a significantly larger thermal mass, (60 x 60 x 35 mm), than the RF test chip with the walls held at ambient temperature. The thickness of the heat paddle and surrounding glass fan-out was modeled to be 25, 50, 100, 150, and 200 µm thick, and each model was run with 50, 100, and 150 W of total power applied at the transistors. The temperature distributions for 50 and 200 µm heat paddles shown below indicates that the overall distribution does not change much, but the maximum temperature was reduced by about 5ºC by increasing the thickness of the heat paddle.

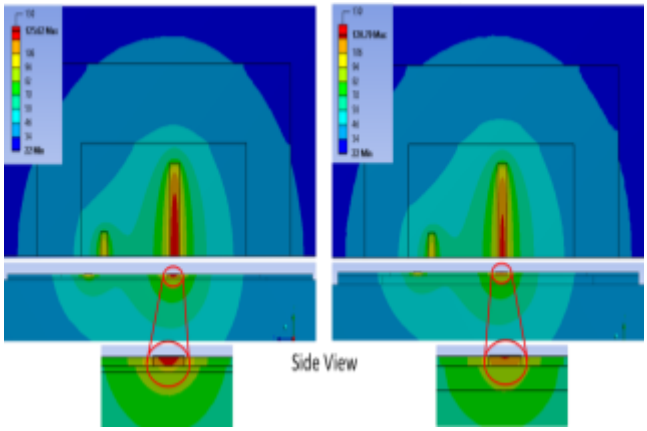


Fig 7. Temperature distribution for the 50 (Left) and 200 µm (Right) Cu heat paddles at 100 W.

The maximum temperature always occurred at the center of the large transistor area, on the top of the GaN layer. Due to the large thermal conductivity of SiC and Cu there was significant spreading within these layers, but the spreading within the glass remained similar across designs. The maximum temperature for each of the thicknesses at each power level is shown below in Fig 8. Although the temperature decrease is small, significant additional temperature reduction can be achieved by increasing the X-Y area of the heat paddle, which will be part of future research.

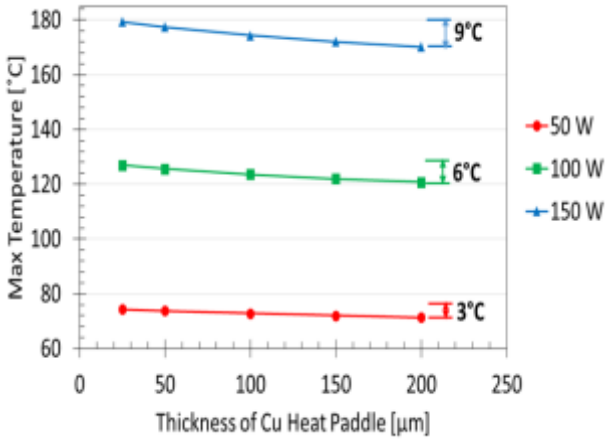


Fig 8. Maximum temperature plotted against the heat paddle thicknesses, (25, 50, 100, 150, 200 µm) for each power applied (50, 100, 150W), and showing the change in temperature between 25, and 200 µm for each power level.

4a. Fabrication of LFO and GFO Packages

The process flow for the laminate fanout package is listed below.

1. Etch or pattern plate copper heat spreader structures on copper foil
2. Form cavities in laminate and prepreg layers to accommodate the copper heat spreaders
3. Integrate the copper heat spreaders on copper foil with the laminate and prepreg using a hot press
4. Pick and place die (with copper bumps) on heat spreader structure and bond using die attach adhesive
5. Laminate dry film polymer dielectric to encapsulate the die and fill the cavity to die gaps
6. Planarization of the surface to expose the copper bumps on the die
7. Semi-additive process (SAP) to form RDL traces and complete the die to package interconnections

The fabrication process started with a thick copper foil to form the heat spreader slugs. Dry film photoresist was laminated onto both sides of the copper foil at 110^0C, and UV exposed for 12 seconds. The backside resist on the copper foil was flood exposed to prevent any etching, and the top side was patterned using a photomask consisting of large rectangular slugs to accommodate die attach. The heat spreaders were designed to be slightly larger than the dies to allow for placement tolerance and bonding. The photoresist was developed by using a spray tool with sodium carbonate solution at a temperature of 80^0C, followed by subtractive copper etching. The final copper thickness was measured to be about 25µm on the base foil with 100µm tall Cu slugs. After the copper slug fabrication, the remaining photoresist wass removed.

The second step of fabrication involved forming cavities in the organic laminate and bondply layers to accommodate the copper slugs. Low dielectric loss laminates and bondply was used to support the high frequency performance needs of the power amplifier package. Cavities were formed in 76µm thick Rogers 2929 bondply film and 120µm thick Rogers 4835 laminates. Both mechanical routing and laser ablation were used to form the cavities. The next step involved hot press lamination to attach the copper slug layer to the laminate using the bondply as the bonding adhesive.

For the placement of the silicon die in the cavities on top of the copper heat spreaders, a chemical desmear process was utilized to clean the surface of the copper heat spreader structure of any polymer residues from the lamination process. Then, solder was dispensed onto the copper slugs at thicknesses between 18 to 22 µm. The die were then placed into the cavities and bonded to the copper heat slugs using a solder reflow process.

Following die placement and bonding, redistribution layers (RDL) were patterned onto the top side of the substrate to form the interconnections to the die pads. Since test die with plated copper microbumps were used, a layer of 20µm thick ABF (GX-92) was laminated on the panel using a vacuum lamination process at 100°C. This ABF layer flows and fills the cavity to die gap as well as providing encapsulation over the copper bumps on the die surface. The ABF was then cured in an oven at 180°C for one hour. The surface of the copper bumps was then exposed by using a new fly cut planarization tool from Disco Corporation, Japan. To form the electrical interconnections to the die bumps, a semi-additive metallization process was used, starting with electroless copper seed layer deposition on the ABF layer, followed by dry film photoresist lithography and copper electroplating to form the interconnects.

A similar process flow was applied to glass substrates, with cavities being formed in the glass by laser or wet etching processes. For the first set of glass panels, the copper slug structures were not integrated, and the back side of the die was bonded to a glass layer. The lower CTE of glass and much higher modulus compared to organic laminates resulted in much lower warpage for glass. The low dielectric loss and hermetic nature of glass is also ideally suited to the high frequency performance needs of the power amplifier package. The fabrication process conditions were optimized for both substrates in order to have an accurate comparison.

4b. Fabrication Results

Both laminate panels with integrated copper heat spreaders and glass panels without the heat spreaders were fabricated using the same test die. Shadow Moire measurements of identical structures in glass and laminate panels indicated an approximately 3x reduction in warpage for the glass compared to the laminate, due to better CTE matching to the IC as well as the higher elastic modulus. The glass panels also showed a 3x improvement in dimensional accuracy with cavity location shift of about 2µm, while organic cavities showed >6µm shift. The initial laminate substrates that were fabricated with embedded die on copper heat spreaders showed both global as well as local warpage, which casued sever challenges in the fly cut planarization process to expose the die bumps, as shown in Figure 9.

Figure 9. Laminate fanout (LFO) panel with embedded die on copper heat spreaders in selected sites, showing warpage induced planarization challenges.

However, selected test sites were successfully fabricated with RDL connecting to exposed die bumps, with integrated heat spreaders below the die to allow for efficient heat dissipation. A top view of a completed LFO package is shown in Figure 10. As seen in the figure, co-planarity challenges will need to be further addressed in the future by design and process optimization.

Figure 10. Completed LFO Package with Embedded IC (75um Thick) on 100um Thick Copper Heat Spreader

Glass fanout packages without the heat spreaders were also successfully fabricated, and a more detailed description of this process has been reported by the authors. Top view and cross-section images of the glass fanout (GFO) packages are shown in Figure 11.

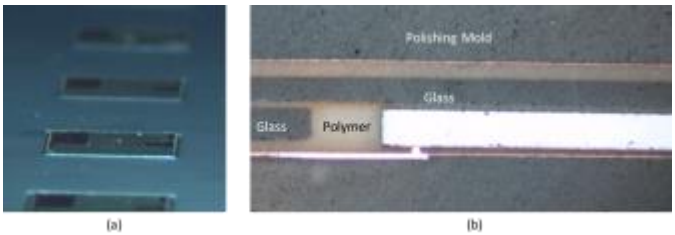


Figure 11. (a) Top View and (b) Cross-section of Glass Fanout (GFO) package.

5. Conclusions

This paper demonstrates for the first time an ultra-thin, panel laminate fan-out (LFO) and glass fan-out (GFO) packages with embedded copper heat spreaders and electromagnetic shields for packaging high power RF ICs in much smaller form factors and at potentially much lower cost than current ceramic and metal flange packages. This unique double sided package addresses the thermal dissipation requirements of 30-100W power amplifiers by bonding the IC directly to a large copper heat spreader embedded in the substrate, using high thermal conductivity die attach paste. It also addresses the RF, microwave and mm-wave performance requirements by utilizing low loss tangent glass and polymer dielectrics, as opposed to lossy epoxy dielectrics or mold compounds. The combination of glass and high temperature polymers also enables superior harsh environment reliability with built-in stress buffer layers to mitigate the CTE mismatch induced stresses from large copper thermal structures. A 5 µm thick polymer liner reduced the stress in glass from 120 MPa to 80 MPa. Further increase in stress-buffer layer thickness to 15 microns reduced the glass stress by more than 50%, to 60 MPa. For effective EMI shielding, various geometries of copper trenches and copper via arrays were modeled for their shield-effectiveness. For a source-victim separation of 0.2 mm, copper trench width of 40 microns was found to create an isolation level of ~60 dB. Laminate and glass substrates were compared for their warpage behavior through finite element modeling, and verified after fabrication. It was observed that glass demonstrated not only a 3x dimensional accuracy improvement but also a 3x warpage improvement both locally and globally.

In summary, the new panel based high power fanout packages demonstrated in this paper represent a compelling new platform for future multi-chip RF and mm-wave high power module integration.

6. Acknowledgments

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References

[1] Wolf, J. A., Peterson, K. A., Vianco, P. T., Johnson, M. H., and Goldammer, S. (*2011*) Robustness and Versatility of Thin Films on Low Temperature Cofired Ceramic (LTCC). International Symposium on Microelectronics: FALL 2011, Vol. 2011, No. 1, pp. 000559-000565.

[2] M. A. Girardi, K. A. Peterson, and P. T. Vianco (*2016*) LTCC Thick Film Process Characterization. Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT): May 2016, Vol. 2016, No. CICMT, pp. 000142-000150.

[3] James Kupferschmidt, Michael Girardi, Brent Duncan, and Daren Whitlock (*2014*) Determination of LTCC Shrinkage Variations from Tape Manufacturer to Consumer. International Symposium on Microelectronics: FALL 2014, Vol. 2014, No. 1, pp. 000668-000672.

[4] M. A. Girardi, K. A. Peterson, P. T. Vianco, R. Grondin, and D. Wieliczka (*2014*) Laser Ablation of Thin Films on LTCC. International Symposium on Microelectronics: FALL 2014, Vol. 2014, No. 1, pp. 000677-000686.

[5] G. E. Ponchak, C. Donghoon, Y. Jong-Gwan, and L. P. B. Katehi, "The use of metal filled via holes for improving isolation in LTCC RF and wireless multichip packages," Advanced Packaging, IEEE Transactions on, vol. 23, pp. 88-99, 2000.

[6] "TriQuint TGA2814 " in *3.1-3.6 GHz Power Amplifier*, ed: TriQuint, 2013, p. 13.

[7] S. Nakamura, "GaN Growth Using GaN Buffer Layer," *Japanese Journal of Applied Physics,* vol. 30, p. 3, 1991.

[8] J. Cho, E. Bozorg-Grayeli, D. H. Altman, M. Asheghi, and K. E. Goodson, "Low Thermal Resistance at GaN-SiC Interfaces for HEMT Technology," *IEEE Electron Device Letters,* vol. 33, p. 3, 2012.