

Analysis Of System-Level Reliability Of Single-Chip Glass BGA Packages With Advanced Solders And Polymer Collars

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Abstract— Emerging high-performance computing systems have been aggressively driving advances in packaging technologies to meet their escalating performance and miniaturization needs. Large, high-density 2.5D silicon interposers have gained momentum with the recent split-die trend but face critical reliability challenges at board-level that are addressed by introducing an additional organic BGA package between interposer and board. Glass substrates have emerged as a promising alternative owing to the superior electrical properties, sub-5 μm lithographic capability and tunable CTE of glass that enables direct SMT assembly to mother boards among other advantages.

This paper investigates board-level reliability of single-chip glass BGA packages, 18.5mm x 18.5mm in body size and 100 μm in thickness at 400 μm BGA pitch. A parametric finite-element analysis was performed to extract the optimum glass CTE for balanced chip- and board-level reliabilities. Innovative doped solder materials and strain-relief mechanisms were evaluated to improve board-level reliability with minimum system-level impact. Daisy-chain test vehicles with low (3.3ppm/K) and high (9.8ppm/K) CTE glass substrates were fabricated and assembled at chip and board levels by Cu pillar thermocompression bonding and standard SMT reflow, respectively. Assemblies with different BGA solder alloys, SAC105, SAC305 and Indium's Mn-doped SACmTM, were subjected to thermal cycling test according to JEDEC standards. Comprehensive failure analysis was performed to evaluate fatigue life improvements with advanced interconnection materials and conclude on scalability of glass substrates for high-performance applications.

Keywords- system-level reliability; glass BGA packages; doped solders; thermal cycling test; finite-element simulation; polymer collars

I. INTRODUCTION

Demands for thinner consumer electronic products have led the trend for package thickness reduction. Such reduction exacerbates substrate warpage and degrades SMT assembly yield and reliability. Further, increasing functional densities in emerging applications are driving the need for greater I/O counts and, subsequently for larger die sizes at finer I/O pitches. Current packages are in turn expected to migrate to sizes larger than 20 mm x 20 mm with progressive reduction in chip-level pitch to below 30 μm . Silicon interposers have gained momentum in high-

performance split-die applications as they satisfy sub-5 μm lithographic design rules required for high-density die-to-die interconnections. These low-CTE interposers frequently exceed 30mm x 40mm in body size but still have to be mounted onto a PCB, displacing CTE mismatch to board level. To accommodate the increase in I/O count, the BGA pitch also needs to reduce, further aggravating solder strains, and bringing unprecedented challenges for board-level thermomechanical reliability.

There have been various interconnection structures designed for strain relief to address the aforementioned challenges. These are mainly compliant interconnection techniques like micro-spring interconnections [1], multi-path fan shaped interconnections [2], printed silicone bumps [3], bump-on-polymer structures [4], embedded solder balls [5], double-ball wafer-level packaging [6] etc. to improve the fatigue life of the package. In addition, extensive research on SMT-compatible solutions for enhanced board-level reliability has been carried out at Georgia Tech's PRC with demonstration of copper micro-wire arrays [7]. Another promising mechanism for strain-relief that has been demonstrated is the use of reinforced polymer collars. They are reported to enhance the thermal cycling reliability by 30-50% [8].

Further, different solder compositions greatly affect its plastic deformation and can be used to improve the fatigue life. Solders like SAC305 with higher Ag content have better thermal cycling performance than solders with lower Ag content due to their higher yield strength and modulus [9]. However, solders with lower Ag content have better drop performance due to their ability to absorb shock. Therefore, higher drop performance can be achieved only at the cost of fatigue life. Further advances in solder interconnection materials are required in order to balance the thermal cycling and drop test reliability for consumer applications. Recently, solders doped with Mn (SACmTM) developed by Indium Corporation enable superior thermal cycling performance comparable to SAC305 by constraining the intermetallics (IMCs) growth and stabilizing the microstructure without compromising its drop test reliability [10, 11]. However, SACm alloy is limited in its applicability only to pitches above 500 μm .

The current approach to achieving board-level reliability with large, low-CTE interposers, however, consists of the addition of a package layer between

interposer and PCB [12]. This increases thickness and parasitics and adds to the system cost. A novel 2-level packaging solution enabling direct, SMT interconnection of large and thin 2.5D packages to the board is highly sought after to address this grand challenge.

Glass substrates have emerged as a promising alternative to silicon interposers for 2.5D applications owing to their superior electrical properties, lower insertion losses, large area panel-based processability and micron-scale lithographic capability, at low cost. Further, glass has tailorable CTE (3.3-9.8ppm/K), high dimensional stability and high modulus, hence can mitigate warpage introduced by thickness reduction. The tailorable CTE also provides design flexibility to optimize chip- and board-level reliabilities. With glass, the desired 2-level hierarchy can therefore become possible. Research carried out at Georgia Tech's Packaging Research Center on the effect of polymer collars have demonstrated superior drop performance of 18.5mm x 18.5mm glass BGA package with SAC105 solder at 400 μ m SMT pitch. The addition of collars further enhanced the thermal cycling reliability of the BGA interconnections by 30% [13].

System-level warpage, yield and subsequent reliability were found mostly governed in 2.5D interposer packages by the substrate CTE, package size and thickness and assembly sequence based on the substrate CTE. Taking advantage of its tunable CTE, glass provides a unique design knob to mitigate warpage and balance chip- and board-level reliabilities and achieve direct SMT assembly to the board. While the ideal glass CTE can be extracted through parametric finite element analysis for any given package configuration, only glass with low (3.3ppm/K) and high (9.8ppm/K) CTEs is readily available today. Advanced interconnection materials such as doped solders and polymer collars were, therefore, introduced to further improve board-level reliability with minimum system-level impact.

This paper is focused on achieving balanced chip- and board-level reliability with a 2-level hierarchical solution by optimizing the design of ultra-thin glass BGA packages for system-level thermomechanical reliability through: a) finite element analysis of fatigue life at chip and board levels as a function of glass CTE; b) validating the models with focused reliability studies of low- and high-CTE glass package assemblies; and c) using innovative doped solder materials such as Indium's Mn-doped SACmTM alloy and strain-relief mechanisms to extend board-level reliability to larger body sizes and give more design flexibility. These approaches provide a unique solution for enhancing board-level thermomechanical reliability while extending the capabilities of conventional solders for direct package-to-board interconnections. They provide a unique combination of strain-relief without adversely impacting chip-level reliability, thus potentially extending board-level reliability to larger and advanced packages. Modeling for chip- and board-level reliability as a function of glass CTE, test vehicle fabrication, assembly and thermomechanical reliability characterization at board level of 18.5mm single-

chip glass BGA packages are discussed in detail in view of system-level impact.

II. TEST VEHICLE DESIGN AND FABRICATION

A. Daisy-Chain Test Die

Daisy-chain test vehicles (Figure 1), 10mm x 10mm in size, with 5448 I/Os arranged in four staggered peripheral rows at 80/40 μ m pitch and a central area array at 150 μ m pitch were used in this study. The silicon test wafers were 300mm in size and were fabricated by Advanced Semiconductor Engineering Inc. (ASE). The wafers were plated with Cu in a dogbone wiring structure and bumped with standard Cu pillars. The copper pillar interconnections were 28 μ m in diameter with 17 μ m copper height, a Ni barrier layer of 3 μ m and a SnAg solder cap, 17 μ m in height. Test dies, 100 μ m and 200 μ m in thickness were used to assess the effect of die thickness.

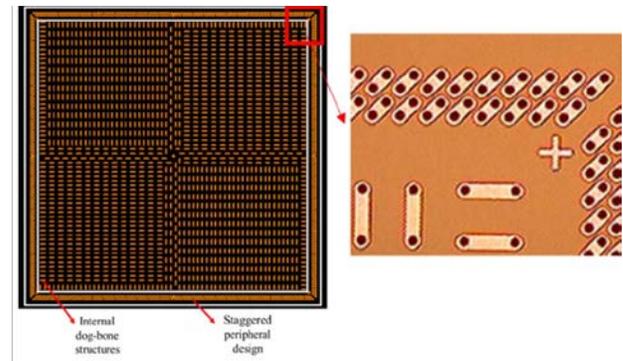


Figure 1. Daisy-chain test die: a) design and b) optical image of a bumped corner (Image courtesy of ASE).

B. Glass Substrate Fabrication

Glass substrates, 18.5mm x 18.5mm in size, with the die footprint on the top side, and a 45 x 45 area array of daisy-chain BGA interconnections on the bottom side is shown in Figure 2. Due to the absence of through-package-vias (TPVs), the chip- and board-level daisy chains are not connected to each other. The design consists of four metal layers, with a dummy mesh pattern in the inner layers for adequate Cu coverage and realistic warpage representation. The substrate was fabricated using a semi-additive process for low- and high-CTE glass on 6 inch x 6 inch panels. The glass core, 100 μ m in thickness, was laminated with 17.5 μ m-thick dielectric layers. The Cu dogbone structures were defined through double-side lithography processes using dry-film photoresist, 10-12 μ m-thick formed by electrodeposition. The photoresist was then stripped and the electroless copper seed layer was etched. The double-side process was repeated again for lamination of dielectric build-up layers. The daisy-chain patterns on the die and BGA sides were simultaneously formed by double-side Cu electrolytic plating. Further, a solder-mask defined (SMD) dry film resist (15 μ m) by Hitachi Chemical was applied as a passivation layer to define landing and probing pads. Surface finish of electroless palladium autocatalytic gold

(EPAG) was plated on the Cu pads by Atotech GmbH with a production-controlled process. The cross-sectional expanded view of the substrate is shown in Figure 3. The substrate stack-up summary is recapped in Table I.

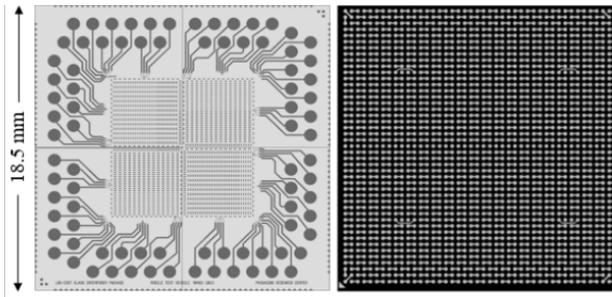


Figure 2. Glass substrate test vehicle design on (left) the die side, and (right) the BGA side.

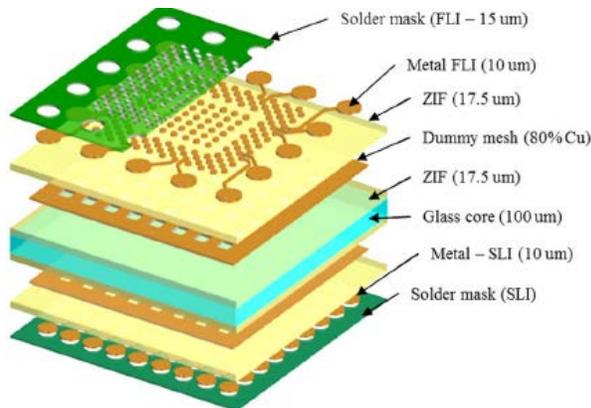


Figure 3. Schematic of 18.5mm x 18.5mm 40metal layer glass substrate.

C. PCB Board Design

The backside of the glass substrates consists of 2025 solder balls at 400 μ m pitch, divided in a network of 52 daisy chains. A single-layer PCB was designed to match the daisy-chain pattern, including four corner circuits and 48 inner chains as seen in Figure 4. The copper pads were non-solder mask defined (NSMD) with a surface finish of electroless nickel electroless palladium immersion gold (ENEPIG).

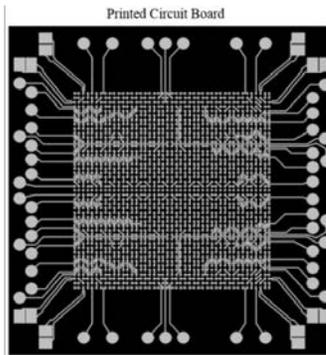


Figure 4. Daisy-chain interconnection design of PCB with probing pads.

Table I. Summary of substrate stack-up materials and design rules

Parameters	Description
Substrate core	Low- & high-CTE glass
Build-up layers	17.5 μ m/17.5 μ m
Solder Resist	15 μ m - SMD
Metal layers	4ML with 80% Cu coverage on inner dummy
Surface finish	EPAG (Atotech Germany)
BGA	250 μ m @ 400 μ m pitch (Paste printed)
Solder	SACm™, SAC305, SAC105 (Indium)
Die thickness	100 μ m, 200 μ m
Underfill	50 μ m

III. FINITE-ELEMENT MODELING

Finite-element models were created to perform a parametric study on fatigue life as a function of glass substrate CTE for a direct-SMT on board package. Modeling was done in ANSYS™ 15.

A 2D model with half-symmetry of a 100 μ m-thick glass package was created with chip- and- board-level assemblies. The geometry includes the silicon die, copper pillar interconnections, polymer dielectric layers, glass substrate, copper redistribution layers assembled with SAC105 solder on the PCB side (Figure 5). A 2.5D or 3D model would be ideal for accurate results. However, 2D models with plane strain approximation are sufficient for this parametric study of comparing the thermal cycling reliability for different glass CTEs. The die-substrate-PCB assembly represents a cut along the diagonal with symmetry boundary conditions at the center. The node at the left bottom was fixed in the y-direction to prevent rigid body motion. The mesh was refined at the solder and thin layers. The mesh was coarser away from the critical regions and the number of elements as compared to the thickness was built to effectively evaluate fatigue life. An example of the model mesh is as shown in Figure 6. Anand's model was used for the modeling of solder as a viscoplastic material.

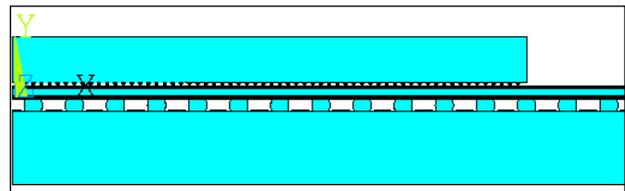


Figure 5. Example geometry in modeling. Two-dimensional geometry represents a cut along the diagonal of the package with symmetry at the left.

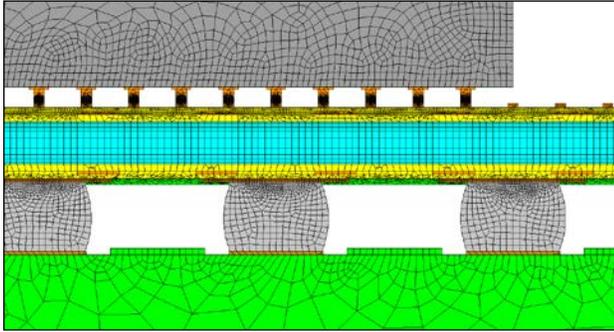


Figure 6. Example mesh used in modeling for thermal and mechanical analysis.

Coupled thermal-structural finite-element models were constructed to predict the fatigue life of the solder joints and provide assembly process guidelines for balanced reliability. The modeled structure was initially subjected to a temperature drop from 260°C to 25°C, simulating the cooling of SMT reflow process. JEDEC standards (JESD22-A106B) were followed that define five thermal cycles between -40°C and 125°C for fatigue life evaluation. The ramp-up and ramp-down temperatures as well as dwell time at the temperature were fifteen minutes each emulating real-time thermal cycling. The model was solved and the equivalent plastic strain range in the corner joint was extracted after cycling and used as damage metrics to predict the fatigue life of the interconnection for chip- and board-level assemblies. The fatigue life of solder joints was estimated using the conventional Coffin-Manson equation [14] as well as Engelmaier-Wild fatigue model [15, 16]. The predicted values have been tabulated in Table II with chip- and board-level assembly for low- and- high-CTE glass with 100 μ m and 200 μ m dies. Figure 7 shows the plastic strain distribution of the outermost solder joints in the Cu pillar as well as BGA interconnections.

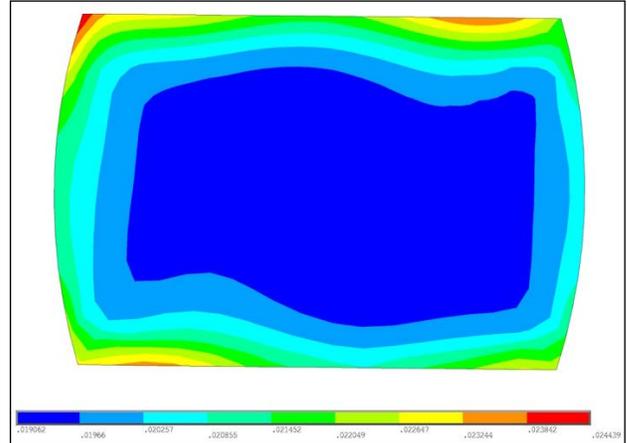
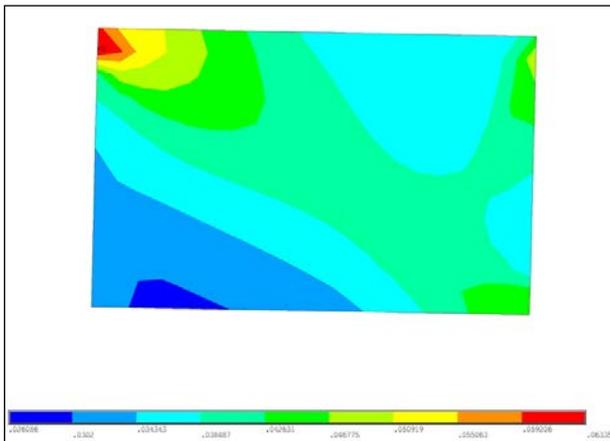


Figure 7. Plastic strain distribution of outermost solder joint at chip-level (top) and board-level (bottom)

Based on the fatigue life models, all package configurations would survive over a 1000 cycles regardless of glass CTE, satisfying JEDEC reliability standards. Model predictions depicted that the chip-level fatigue life exceeded 1000 cycles by a large margin. There was no cross-over between the chip- and- board- level reliability as a function of substrate CTE. As expected, the board-level fatigue life of high-CTE substrates was predicted to be better than that of low-CTE substrates. However, the low-CTE glass packages at board-level barely passed 1000 cycles. Therefore, board-level reliability is a major issue and needs to be addressed. It can be seen from the predictions that the substrate CTE has a larger impact on board-level reliability as compared to that of chip-level. Since only glass with low (3.3ppm/K) and high (9.8ppm/K) CTEs is readily available today, advanced interconnection materials such as doped solders and polymer collars were introduced to further enhance board-level reliability with minimum system-level impact. Moving to 2.5D architectures, the chip- and board-level reliabilities of the system is expected to deteriorate further. This is because even though the board-level interconnection pitch is targeted to be coarser for 2.5D packages, the increase in package size and decrease in chip-level interconnection pitch will adversely impact the board-level fatigue life. Given that, low-CTE substrate packages may not pass JEDEC reliability standards at board-level. In order to balance the reliability, the optimum glass CTE can be extracted from the model similar to the plot in Figure 8. Based on modeling predictions, conclusions can be made on the need to alter the assembly process and sequence by moving towards higher CTEs or the necessity of advancing to compliant interconnections.

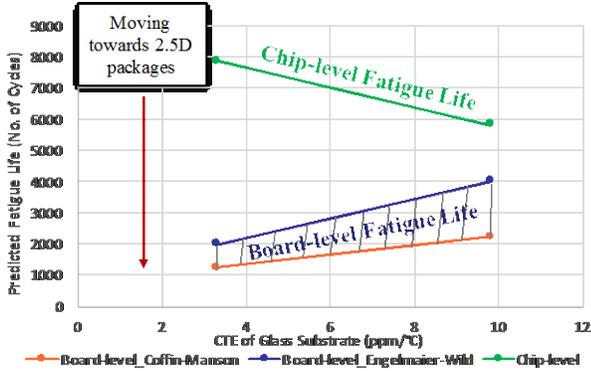


Figure 8. Fatigue life vs. CTE using Coffin-Manson and Engelmaier-Wild models

Table II. Predicted fatigue life for chip- and board-level assembly using Coffin-Manson and Engelmaier-Wild models

	Chip-level Fatigue Life	Board-level Fatigue Life	
	Coffin-Manson	Coffin-Manson	Engelmaier-Wild
Low-CTE	7856	1205	1926
High-CTE	5815	2158	3871

IV. ASSEMBLY AND YIELD EVALUATION

Test dies, 100 μ m and 200 μ m in thickness were assembled by dip-flux thermocompression bonding process using a semi-automatic Finetech Fineplacer Matrix flip-chip bonder with a placement accuracy of $\pm 3\mu$ m. The stage temperature was at a constant of 100 $^{\circ}$ C, the tool head peak temperature on the die side was 360 $^{\circ}$ C with a heating rate of 6K/s and a pressure of 0.9MPa was applied throughout the process. The bonded assemblies were then underfilled with the Namics Corporation 8410-219 material through dot-dispensing process manually. The underfill was then cured at 165 $^{\circ}$ C for two hours.

After chip-level assembly, BGA balling was done at panel-level with SAC305, SAC105 and SACmTM solder alloys using an optimized paste printing process. 9 samples with SACmTM solder alloy that were spin-coated with circumferential polymer collars [17] were used for thermal cycling test in order to compare the effect of this strain relief mechanism on fatigue life. The number of samples in test for each configuration is listed in Table III.

After laser dicing, the glass packages were then assembled on PCBs using a standard pick-and-place reflow process. This pick-and-place process was performed using the same Finetech Matrix fineplacer using no-clean tacky flux. The optimized reflow conditions using standard SMT process was optimized to minimize voiding. A summary of the assembly process is shown in Figure [13].

Electrical measurement of the daisy-chain resistances was performed to evaluate yield. The overall balling yield was of 85%, with lower yield in high-CTE substrates due

to increased warpage after chip-level assembly. The yield after SMT assembly was measured to be 90%. A total of 32 low-CTE and 4 high-CTE samples were chosen for thermal cycling. The number of high-CTE samples were limited due to yield loss. It is important to optimize the TCB conditions to prevent yield loss due to assembly warpage based on substrate CTE.

Table III. Sample distribution for all test configurations

Package Type	BGA Solder	# of Samples in Test
Low-CTE glass (with 200μm-thick die)	SACm TM	6
	SACm TM with collars	6
	SAC305	6
	SAC105	5
Low-CTE glass (with 100μm-thick die)	SACm TM	5
	SACm TM with collars	5
	SAC305	3
	SAC105	4
High-CTE glass (with 100μm-thick die)	SACm TM	4 (yield loss due to warpage)

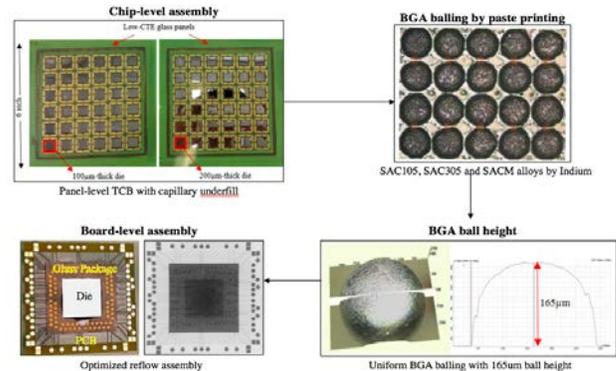


Figure 9. Summary of chip- and board-level assemblies.

V. THERMAL CYCLING RELIABILITY TEST

Thermal cycling was performed following the JEDEC JESD22-A104D standards that define five temperature steps between -40 $^{\circ}$ C and 125 $^{\circ}$ C with a dwell time of 15 minutes at each extreme, with one cycle an hour. The resistance of each test vehicle was monitored every 100 cycles. The failure criteria were defined as an increase in the resistance by 20% or an electrically open daisy-chain. All samples passed 1000 cycles with stable daisy-chain

resistances, regardless of glass CTE and solder alloys. The low-CTE samples failed in the range of 1100-1800 cycles while the high-CTE cycles passed 2600 cycles and are still in test. These results correlate well with modeling predictions.

A. Failure Distribution

Failed samples were characterized for void-detection using X-ray analysis. The sample failure distribution for all daisy-chain test vehicles are plotted in Figure and Figure for the 200 μ m-thick and 100 μ m-thick dies, respectively. Samples with excessive voiding failed earlier than expected. The average failure distribution for the 200 μ m-thick die packages are as follows - 1350 cycles for SAC105, 1550 cycles for SAC305, 1450 cycles for SACm™ without polymer collars and 1600 cycles for SACm™ with polymer collars. The number of cycles to failure for the 100 μ m-thick die packages were similar to that of 200 μ m-thick dies, but with a broader failure distribution. The thermomechanical reliability results were as expected – Soft solder SAC105 having the least fatigue life, hard solder SAC305 with superior TCT reliability and SACm™ exhibiting similar fatigue behavior as that of the higher Ag content solder, SAC305. Additionally, samples with polymer collars improved the fatigue life. A 25% increase in fatigue life can be achieved with advanced interconnection materials for a direct SMT assembly glass package with finer BGA pitches of 400 μ m.

B. Optical Inspection

The failed samples were underfilled to prevent solder smearing during polishing and molded in an acrylic resin for cross-sectioning to identify the predominant failure modes. Inspection of the BGAs in individual rows indicated that the defects occurred mainly in the outer rows and corner circuits, as expected; since the BGAs are less prone to failures when they are closer to the neutral point. Figure shows the different failure modes identified in the BGAs after optical inspection. Two main types of failure modes were established. Warpage-related failures can be seen from the non-wets and stretched solders while fatigue failures can be observed with cracks initiating close to the IMC-to-solder interface on the corner BGAs. Early failures were mostly due to warpage-related defects at around 1200-1300 cycles while the fatigue defects failed at around 1500-1600 cycles. Warpage measurements after BGA balling and after board-level assembly reported in [13], and as shown in Figure indicate highest warpage in low-CTE samples with 100 μ m-thick dies. This explains the broader failure distribution observed in these assemblies, with, on average, more warpage-related defects than in other failed packages.

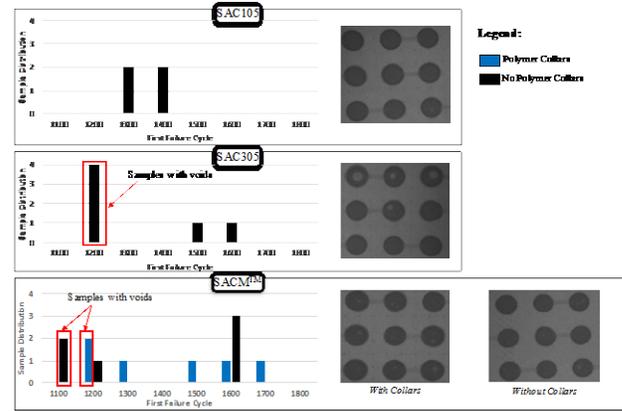


Figure 10. Failure distribution for low-CTE glass packages with 200 μ m-thick die

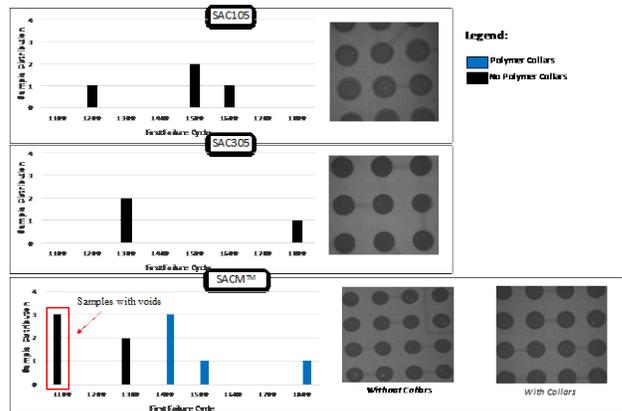


Figure 11. Failure distribution for low-CTE glass packages with 100 μ m-thick die

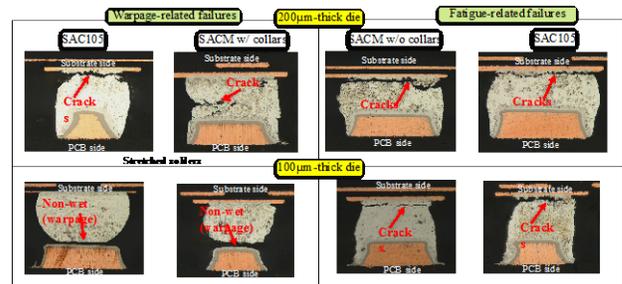


Figure 12. Optical characterization of cross-sections of failed assemblies with SAC105, SAC305 and SACm™ BGAs for identification of failure modes.

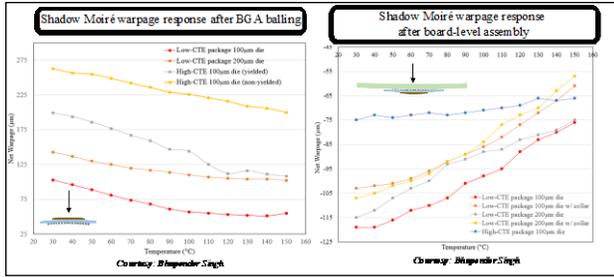


Figure 13. Shadow-Moiré warpage response after BGA balling (left) and after board-level assembly (right).

I. SUMMARY

This paper successfully demonstrates system-level reliability of a single-chip glass BGA package, 18.5mm in body size, meeting thermomechanical reliability standards. Using a parametric study, the effect of glass CTE on fatigue life was evaluated. While the ideal glass CTE can be extracted through parametric finite element analysis for any given package configuration, only glass with low and high CTEs is readily available today. Advanced interconnection materials such as Novel Mn-doped SACm alloy developed by Indium Corporation and polymer collars were, therefore, introduced to further improve board-level reliability with minimum system-level impact.

Finite-element models were developed to predict the fatigue life as a function of glass CTE. Based on model predictions, it can be seen that chip-level reliability exceeds the JEDEC standards of thermomechanical reliability by a large margin. On the other hand, board-level reliability is more sensitive to substrate CTE. As we move to larger package sizes, high-CTE is an ideal solution as long as it doesn't degrade chip-level reliability. Daisy-chain test vehicles, 18.5mm x 18.5mm in body size and 100µm-thick glass substrates with low (3.3ppm/K) and high (9.8ppm/K) CTEs were assembled at chip-level with silicon test dies, 100µm and 200µm in thickness by thermocompression bonding followed by capillary underfilling. The assembled package substrates were then by BGA balled using paste-printing at panel-level and laser diced. A standard SMT reflow process was used to assemble the package onto the PCBs. Experimental results for board-level thermomechanical reliability correlate well with the model predictions.

Failure distribution analysis and optical characterization was performed to evaluate thermal cycling reliability. All samples passed the JEDEC standard of 1000 cycles, regardless of glass CTE and solder alloy. As expected, SAC105 failed the earliest at 1300 cycles and the Mn-doped SACm alloy exhibited superior fatigue life of 1450 cycles comparable to that of SAC305 with 1550 cycles. Furthermore, samples with polymer collars showed better performance with 1600 cycles to failure. Optical inspection through cross-sectioning of failed low-CTE samples revealed two predominant failure modes - warpage and fatigue defects. Samples with warpage-related defects failed prior to the expected number of cycles. In best conditions of advanced solder interconnection materials,

the low-CTE samples can survive a maximum of 1600-1800 cycles for a large single-chip glass BGA package. High-CTE glass packages, currently in test at 2600 cycles, are within the model predicted range of 2100-3800 cycles. Even with the best configurations of low-CTE samples, high-CTE samples are shown to present higher fatigue life. There is limited scalability in terms of reliability of low-CTE packages as we move towards 2.5D and 3D architectures. Thus, higher CTE glass may need to be considered for direct SMT assembly to the board.

Further work on warpage mitigation in assembly is ongoing to provide a complete and comprehensive solution for high-performance applications. There is a need to mitigate warpage, optimize the substrate CTE and package thickness through a parametric analysis in order to achieve balanced chip- and- board-level reliability.

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