High Frequency Electrical Performance and Thermo-Mechanical Reliability of Fine- Pitch, Copper - Metallized Through-Package-Vias (TPVs) in Ultra – thin Glass Interposers

Sukhadha Viswanathan*, Tomonori Ogawa**, Kaya Demir, Timothy B. Huang, P. Markondeya Raj, Fuhan Liu,
Venky Sundaram and Rao Tummala, IEEE Fellow
Packaging Research Center, Georgia Institute of Technology,
813 Ferst Dr. NW, Atlanta, GA 30332
*sviswanathan37@gatech.edu
**Asahi Glass Co. Tokyo, 100-8405

Abstract: This paper demonstrates the high frequency performance and thermo-mechanical reliability of through vias with 25 µm diameter at 50 µm pitch in 100 µm thin glass substrates. Scaling of through via interconnect diameter and pitch has several electrical performance advantages for high bandwidth 2.5D interposers as well as mm-wave components for 5G modules. This paper focuses on the assessment of thermo-mechanical reliability, of high aspect ratio TPVs at ultra-fine pitch, metallized using a via–first approach, and the accurate electrical modelling of TPVs and transmission lines with TPVs up to 40 GHz, using ANSYS HFSS™. Test vehicles consisting of through via daisy chain structures were designed and fabricated on 100 µm thick glass, laminated with a 5 µm epoxy dry film polymer on both sides. Fine pitch TPV arrays were subjected to Thermal Cycle Testing (TCT) between -55 °C and 125 °C, and the majority of TPV chains passed 1000 cycles with less than 15% change in DC resistance. The impact of pitch scaling on the reliability was studied by varying the spacing of neighboring TPVs using 3D quarter-symmetric finite element models. A novel approach based on wave dimensional analysis was investigated to accurately capture the electrical parasitics of the vias in mm wave frequency bands. The resistance and inductance of a single signal TPV at 28 GHz were estimated to be 93 mΩ and
60 pH respectively. Using Voltage Standing Wave Ratio (VSWR) calculations, it was shown that smaller via diameters are preferable for transitions from a 50 Ω impedance matched planar to vertical interconnection.

Keywords - Through Package Vias (TPVs), 3D Interposer, Themal Cycle Testing (TCT), Transmission lines (TLs),Voltage Standing Wave Rati (VSWR)

I. Introduction

Increasing demands for bandwidth in high performance computing, 5G communication, autonomous driving, and Internet of Things (IOT) applications have driven the migration to 2.5D and 3D interposers, requiring ultra-fine pitch and low loss vertical interconnections. 3D ICs provide very high data bandwidth due to ultra-short vertical connections at extremely fine pitch, but have not seen widespread adoption due to thermal limits and high through silicon via (TSV) cost. Wafer based 2.5D silicon interposers, first demonstrated by Xilinx, are seen as a stepping stone to true 3D logic–memory connectivity. 3D interposers [1] have been proposed by Georgia Tech to address 2.5D interposer challenges in scaling bandwidth due to the longer interconnections and high trace resistances. Such a 3D interposer structure is also important for 5G modules to interconnect antennas on one side to mm-wave ICs on the other side. Through vias of very small diameters at fine pitch with low electrical loss are a key building block towards 3D interposer realization. Interposer cost reduction has fueled a renewed interest in panel-based interposer packages that can be direct SMT attached to PWBs. Tremendous advances in organic interposers have been demonstrated by Shinko, Kyocera, but organic substrates have fundamental scaling limits in through via and RDL wiring density due to their poor dimensional stability. To address these limitations, the Georgia Tech Packaging Research Center (PRC) has proposed and demonstrated panel scalable glass interposers with side–by–side or double side assembly of ICs in 2.5D and 3D configurations, respectively. This paper focuses on the high performance design and reliable metallization of high density through package interconnections in thin glass interposers. TPVs in glass at larger diameters and pitch have been reported [2], however, this paper reports on the reliability and mm-wave loss of through vias at smaller diameter and pitch.

Reliable copper metallization of fine pitch and high aspect ratio Through Package Vias (TPVs) in glass is challenging due to the high degree of mismatch in Co-efficient of thermal expansion (CTE) between glass (3 ppm/K) and copper (17 ppm/K) as well as poor adhesion due to their contrasting chemical structures, and ultra-smooth surface of glass. Physical vapor deposition (PVD) metallization using an adhesion layer of Titanium or Chromium, followed by deposition of copper has been demonstrated for metallizing glass substrates with TPVs [3]. However, this approach suffers from aspect ratio limits due to line of sight deposition, as well as lack of a stress buffer between Cu and glass.

Reducing the pitch of through vias raises additional reliability concerns due to the close proximity of vias and accumulation of stress from CTE mismatch between copper and glass. Hole formation processes must be controlled to minimize or eliminate the formation of micro-scale defects that could act as failure sites. The development of high throughput metallization processes for high aspect ratio through vias at fine pitch is required for high volume applications. Several TPV formation and metallization processes have been explored in glass substrates, however, there is limited published work on fine pitch TPV metallization reliability and high frequency characterization. This paper presents work on through vias in glass panels and metallized by a high throughput, large panel scalable electro- less and electrolytic copper plating process.

To address the cost and reliability needs, the first part of this paper demonstrates a novel via-first metallization technique, named the primer process, based on high throughput electro-less plating. In this approach, a thin dry film polymer (primer) is first laminated on a bare glass substrate containing TPVs followed by polymer patterning to open the vias for seed layer Cu deposition. Optimization of the primer process for smaller diameter (≤ 25 µm) and fine pitch (≤ 50 µm) vias is highlighted. Arrays of variable length Cu daisy chain TPV structures were fabricated on low CTE (3 ppm/K) glass (Asahi Glass, Japan) using the aforementioned process and assessed by Thermal Cycle Testing (TCT). The primer approach is scalable to smaller diameter TPVs than the via-in-via approach reported earlier since it does not require a second via opening in the polymer filling the TPV [4]. Earlier work on thermo-mechanical reliability of TPVs focused on a pitch larger than twice the via diameter [7]. In this paper, the mechanical stresses experienced by TPVs at an aggressive pitch with 25um via to via spacing is estimated using Finite Element Analysis.

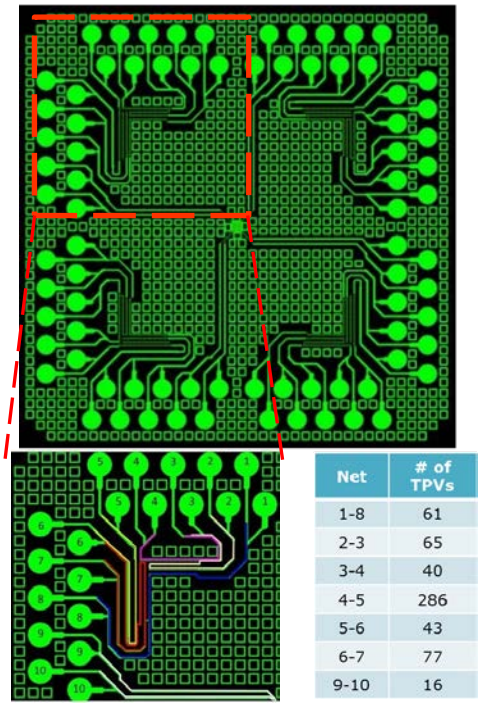
The second part of the paper focuses on high frequency modeling of ultra–short vertical interconnections in 100 µm glass. The most recent report on the electrical characterization of TPVs was on 300 µm thick glass [5]. The authors have used dual via chain, Short–Open circuit via configurations to measure the parasitics of TPVs formed by focused electrical discharge only up to 30 GHz [5][6]. This paper goes beyond the previous published work in identifying the shortcomings of circuit based techniques and proposing an EM wave based approach for the accurate measurement of TPV parasitics up to 50 GHz. The improvement in performance of TPVs with shorter interconnection length in 100 µm thickness compared to thicker glass substrates was validated through 3D EM simulations using the proposed technique.

This paper is organized as follows. Section II describes the fabrication processes used to metallize fine pitch TPVs in 100um glass substrates. The characteristics of thermal stress interaction between copper-plated TPVs was studied using finite element models (FEM) built in ANSYS™ in Section III.A. In addition, the thermal reliability of the TPVs metallized using the primer process was validated through accelerated Thermal Cycle Testing (TCT) up to 1000 cycles and the results are discussed in Section III.B. Preliminary modeling of the high frequency loss of small TPVs up to 40GHz is discussed in Section IV, followed by Conclusions in Section V.

II. Fabrication Process:

A) Primer process for via metallization:

A via–first metallization technique, hereby referred to as the primer process, was used to enable reliable and conformal deposition of copper on 100 µm thin glass with TPVs. For the reliability demonstration of proposed via metallization technique, daisy chain structures of TPVs of 25 µm diameter at 50 µm pitch were initially formed on 100 µm thin glass substrates provided by Asahi Glass Co. The test vehicle design and the fabrication process flow are shown in Fig 1 and Fig 2, respectively.



Net	# of TPVs
1-8	61
2-3	65
3-4	40
4-5	286
5-6	43
6-7	77
9-10	16

Figure. 1 a) Test Vehicle design containing variable length TPV daisy chain structures b) Single coupon design c) No of TPVs in each net

Following through hole formation, both sides of the glass were laminated with 5 µm thin Ajinomoto Build up Film (ABF) GX92P, as an interfacial layer between glass and copper. The polymer layer also serves as a mechanical stress buffer and aids with the handling of ultra-thin glass. Ideally the thin polymer film is expected to tent over the vias, with no flow inside them. But at elevated temperatures of curing after lamination, the polymer is expected to flow inside the vias with low viscosity. Presence of polymer layer on the side wall of TPVs could make the subsequent step of etch patterning difficult. To overcome this issue, the polymer was partially precured before laminating on glass such that the polymer did not flow into the vias, a process which is detailed in another study [8].

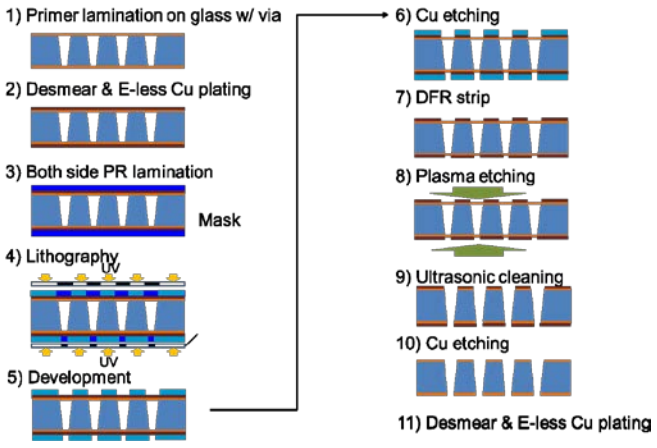


Figure 2. Schematic of primer process using copper etch mask.

Stack Up Dimension	
Solder Resist	15um (Hitachi)
Low Loss Dielectric (Epoxy based polymer)	5 µm
Glass Thickness	100 µm
Low Loss Dielectric (Epoxy based Polymer)	5 µm
Solder Resist	15um (Hitachi)

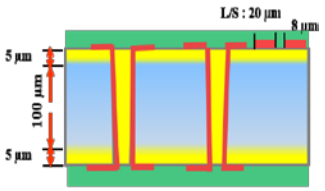


Figure. 3 Stack up dimension of the test vehcile

Following lamination, the next step was to pattern the thin polymer film to open the vias for metallization. Two different processes, one using a copper etch mask as shown in Fig 2 and the other using a photoresist etch mask, were developed and compared for the quality of patterning. The technique of using photoresist left residues on the ABF surface, limiting the full opening of vias. Hence the approach using copper mask was down selected, in which a thin layer of electroless copper was deposited on the polymer after polymer lamination. This process left no residue on the ABF after plasma etching. Fig 4 shows the fully opened TPVs after plasma etching with the copper mask. After the ABF was patterned, a thin seed layer of copper was conformally coated using electro-less copper plating chemistry from Atotech

GmbH, Germany. These preliminary steps appropriately prepare the ultra-thin glass substrate with small diameter, fine-pitch TPVs for the subsequent semi–additive processing steps.

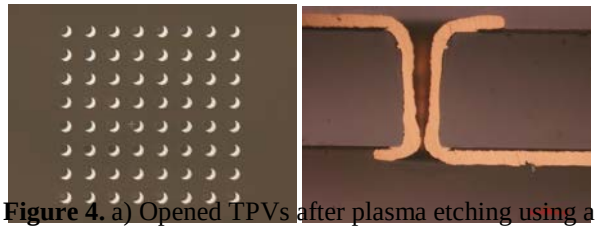


Figure 4. a) Opened TPVs after plasma etching using a copper etch mask. b) Cross section of metallized TPV

The test vehcile consisting of daisy chain TPV structures was fabricated using an optimised primer process and a semi – additive process. The picture of a section of the fabricated sample, captured through optical microscope at 50x magnification, is shown is Fig 5. It can be observed that the via geometry is nearly circular, which is important for good high frequency signal propogation, as discussed in section IV.

III. Mechanical and Thermal reliability of small TPVs at ultra-fine pitch:

A) Mechanical reliability of fine pitch vias

In order to capture the impact of neighboring TPVs on the mechanical reliability, 3D quarter-symmetric finite element models were built as shown in *Fig 6*. Symmetric boundary conditions were applied on inner surfaces whereas periodic boundary conditions were applied on outer surfaces. A standard thermal load cycle of -55 °C to 125 °C was used in the analysis with a dwell time of 15 min at both extreme temperatures. The glass transition temperature of the polymer was chosen to be the stress free temperature of the glass – polymer interface, since the fabrication process flow starts with the lamination of the polymer on both sides of glass. For copper it was chosen as 108 °C based on previous experiments [5].

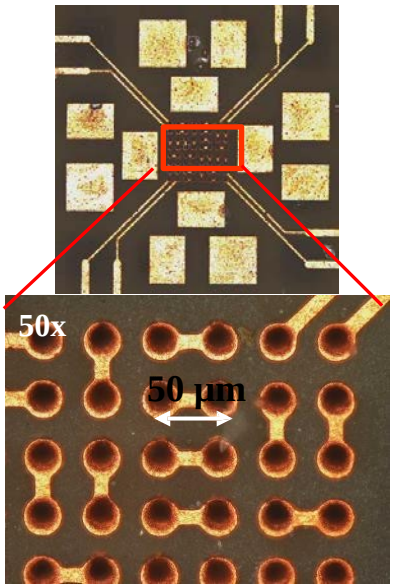


Figure 5. Fabricated daisy chain test structure

The material properties used in the simulation models are listed in Table 1. All materials were assumed to exhibit isotropic behavior. Linear elastic models were applied to glass and polymer, whereas bilinear kinetic hardening model was used for copper with yield strength of 172.3 MPa and hardening modulus of 1034 MPa.

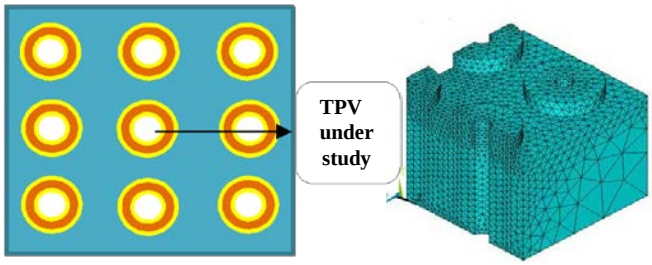


Figure 6. Finite element model for quantifying the impact of elastic interaction: (a) Unit cell for modeling and (b) meshed model of TPV with neighboring vias

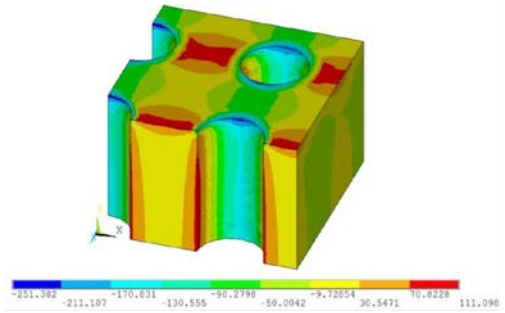
Table 1. Material properties for FEA model.

Material	Elastic Modulus (GPa)	Poisson's Ratio	CTE (ppm/K)	Stress free Temp. (C)
Glass	77	0.22	3.8	162
Copper	121	0.3	17.3	108
Polymer	5	0.3	39	162

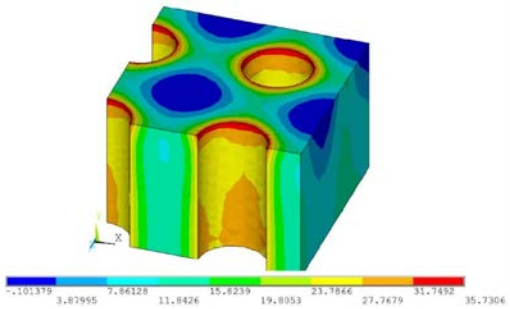
The stresses associated with TPV of 25 µm diameter at 50 µm pitch in a substrate stack up of 100 µm thin glass substrate laminated with 5 µm ABF GX92P polymer on both sides,

were studied. The contour plots obtained in cartesian X direction (σ_{XX}) at -55 °C and first principal stress in glass at 125 °C is shown in Fig 7. Stresses are observed to be intensifying in the x direction, due to the elastic interaction between TPVs. On the contrary, first principal stress is symmetrically distributed around the via locality, resulting in stress free zone surrounding its central region.

Further, the via pitch was varied from 45 µm to 60 µm in steps of 5 µm and the corresponding change in first principal stress at - 55 c is plotted in Fig 8. It is observed that at -55 °C, the stress in glass increases with decreasing via pitch, due to the elastic interaction between neighboring TPVs. However, the maximum principal stress is not significantly impacted by the via pitch, in case of conformal plating of TPVs with 8 µm copper thickness on diameter of 25 µm. Elastic interaction between TPVs is further decreased at 125 °C, which is closer to the stress free temperature of materials used in fabrication.



a)



b)

Figure 7. Contour plots of (a) stress in Cartesian direction (σ_{xx}) (MPa) and (b) 1st principal stress (MPa) in glass for 50 µm pitch.

This study focused on the formation and metallization of TPVs at a pitch of 50 µm, which is twice the diameter. Corresponding analysis of the stress plots indicates that the impact of neighboring TPVs can be considered negligible. Furthermore, the fabrication processes are double sided, which potentially eliminates the warpage that can cause a global strain distribution on the glass panel. As a result, probability of TPV failure can be assumed to be independent of its location on glass.

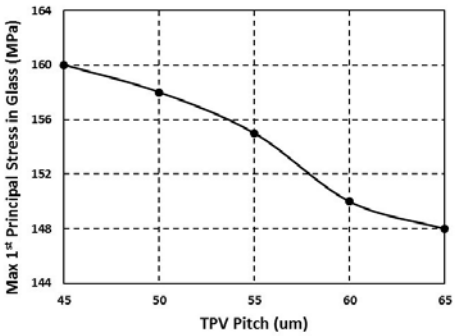


Figure. 8. Change in maximum 1st principal stress in glass for varying TPV pitch.

B) Thermal Reliability Characterization

To estimate the DC resistance of TPV chains and their thermal reliability, daisy chain structures with number of vias varying from 16 to 263 were designed. The thermal reliability characterization consisted of subjecting the test sample to pre-conditioning followed by Thermal Cycle Test (TCT). The pre-conditioning included three steps namely bake, moisture and reflow. First, the fabricated test sample was baked in an oven at 125 °C for 24 hours. This was followed by moisture soak in humidity chamber, based on JEDEC™ Standard 020D.1 Moisture Sensitivity Level 3 (MSL3, 60% RH at 30 °C for 168 hours). However, the available humidity chamber didn't possess the required temperature settings, due to which the sample was subjected to 43 °C, resulting in more rigorous testing than MSL3.Reflow was done three times at peak temperature of 260 °C based on JEDEC standard JESD22-A113F, for pre-conditioning of non – hermetic surface mount devices prior to reliability testing. After pre-conditioning, Thermal Cycle Test (TCT) was performed based on condition B of JEDEC Standard JESD22-A104D. It suggests a temperature range of -55 to +125 °C, in one hour cycles with ramp and dwell times of fifteen minutes each. The sample was periodically inspected and the DC resistance of the variable length TPV daisy chains was measured after preconditioning, 100, 250, 500 and 1000 cycles of TCT. Measurement data is plotted against no of cycles, in Fig. 9.

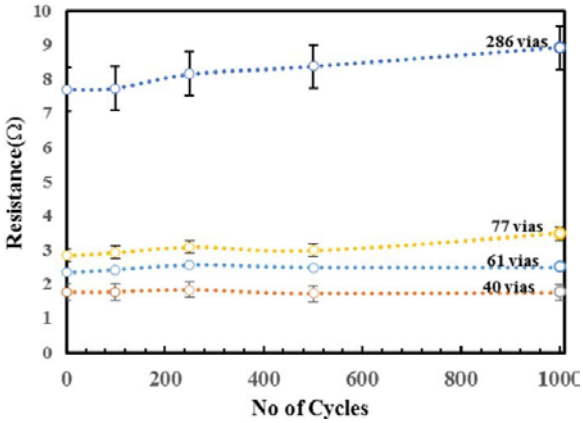


Figure 9. DC Resistance of TPV chains during TCT.

The standard deviation in the resistance amongst daisy chains of the same length was less than 15% in all the varying

lengths of daisy chain structure. The plotted values were obtained, by averaging out the measurement values across 64 similar coupons in the panel. Therefore, the change in resistance was negligible for any individual chain. Cross section was carried out on few TPV chains, one of which is shown in Fig 10. Optical inspection indicate that no apparent delamination or crack is found in the metallized TPVs side walls, validating the mechanical reliability of the primer process for fine pitch TPVs.

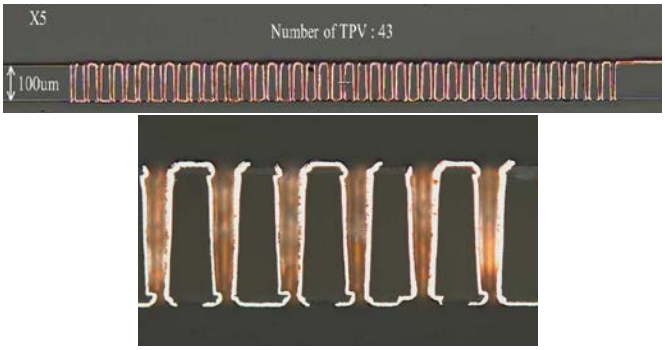


Figure 10. Cross sections of TPV chains in daisy chain formation.

A comparative analysis was done on DC resistance of TPV chains, between the analytical modelling and 1000th cycle data of Thermal Cycle Test (TCT). For the purpose of analytical modelling, TPV chains were considered as circular interconnects, resistance of which is calculated using equation 1.

$$R := \frac{\rho * l}{\pi * r^2} \quad (1)$$

where ρ is considered the resistivity of copper metal, which is 1.68E-8 Ωm, l is the length of the via (130 µm), drilled through the 100 µm thick glass and double sided 5 µm thick polymer, r is the radius of the conformal metal plated via which is the same as the plated metal thickness (8 µm). The TPVs in daisy chain fashion were interconnected through a short planar interconnection of length 50 µm having rectangular cross section. The comprehensive results are plotted in Fig 11. The resistance has direct dependence on the length of the TPV chain, as indicated by the plot in Fig 11.

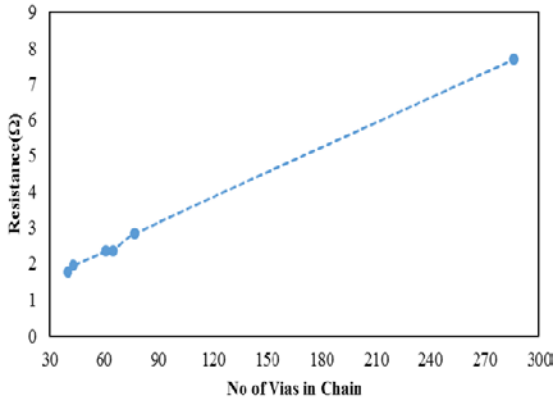


Figure. 11. Simulation of DC resistance of TPV daisy chains of variable length.

The DC resistance of the fabricated daisy chain structures after 1000 cycles of TCT have close correlation with modelling data, marked respectively as ideal and fabricated, in Fig 12. This confirms the reliability of primer process for via metallization. The small deviations are attributed to the varying thickness in plated copper and the copper oxidation in room temperature which affects the accuracy of DC resistance measurement.

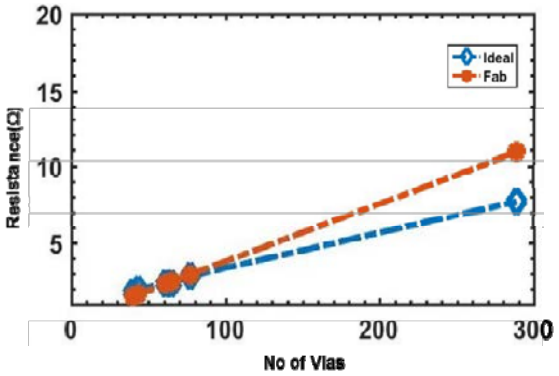


Figure 12. Theoretical and fabricated results for DC resistance of TPV daisy chains.

IV. 3D EM Modelling of TPVs:

A) Estimation of TPV performance using Input impedance method:

The data rate consumption in today's fast paced electronics world has reached a spot, where, even the low parasitics of via transitions in a 3D package, with inductances in ranges of pH has considerable impact on the system speed. In this section, a single signal TPV is studied for its parasitics, namely resistance, inductance and the corresponding insertion loss, using ANSYS HFSS™, a 3D EM simulator. This research proposes a novel methodology, named input impedance technique to estimate the TPV parasitics. The 2D model of the proposed technique is shown in Fig. 13. This technique was accordingly modeled in EM simulator and the results provided detailed insight into the power loss associated with TPVs in glass.

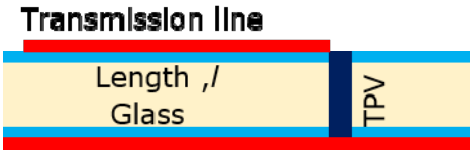


Figure 13. Input Impedance method for estimating TPV parasitics

The proposed methodology consists of estimating the input impedance of the transmission line terminated with Through Package Via(TPV). The impedance, which is estimated through EM simulator follows Equation 2.

$$Zin = Zo\frac{Z_l + j\,Zo\tan\beta l}{Zo + j\,Z_l\tan\beta l} \quad (2)$$

where Zin is the input impedance of the transmission line, which in this case was a micro strip line terminated with TPV, Zo is the characteristic impedance of micro strip, which was 50 Ω and Z_l, is the impedance of the TPVs in GSG configuration, $\beta = 2*\pi / \lambda_{eff}$ is the phase constant associated with the wave traveling at a particular frequency, l is the length of the transmission line. From the known values of Zin, Zo, β and l, Z_l can be calculated, which is the impedance of a single TPV.

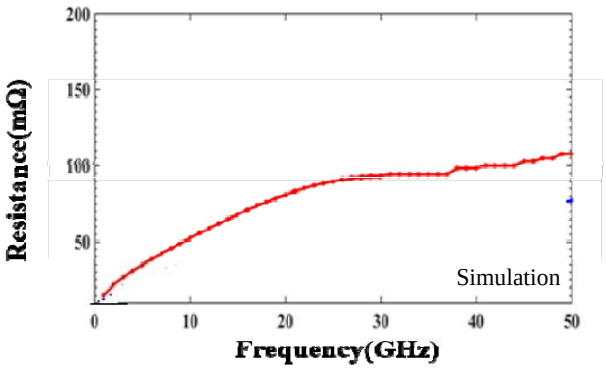


Figure.14 AC Resistance of a signal TPV

Due to the absence of signal return path vias, the real part and the imaginary part of Z_l are considered to be the resistance and the inductive reactance of a single TPV respectively. Fig 14 shows the AC resistance of a signal TPV upto 50 GHz. It seems to exhibit a linear relationship with frequency, attributed to the skin effect, which is more pronounced at higher frequencies. Fig. 15 shows the inductance of the TPV calculated for different aspect ratios of the vias ranging from 0.3 to 1.2, at frequency of 28 GHz for a stack up as shown in Figure 3. It can be observed that as the diameter of the TPV increases, the inductance decreases, which essentially denotes a lower impedance of the TPV. In a microwave circuit, impedance disconuity between the transmission lines and the vias can cause significant power loss due to multiple reflections. One of the widely used parameters to estimate the reflective loss is the Voltage Standing Wave Ratio (VSWR). Reduced value of the VSWR is essential to operate the circuit at high speed. In case of via transitions, lower VSWR can be achieved by proper impedance match of the planar transmission line with the vertical Through – Package-via (TPV). Using the input impedance method mentioned in this paper, it is shown that smaller vias have higher impedance, nearing 50 Ω, for impedance match to the transmission line. Dual via chain structures were designed and modelled in Ansys HFSS™, as shown in Fig 17, to estimate the impact of the via diameter on the performance of the signal transitions.

The length of the metal trace on the top layer was kept at 0.4 mm whereas the bottom metal trace was kept at 1.0 mm. The signal and ground traces in the CPW based dual via chain transition from one metal layer to another through vias. As the diameter of the vias are varied, the center to center via pitch is kept constant at 120 µm. The insertion loss and Voltage Standing Wave Ratio (VSWR) of this structure are plotted in Fig 17 and Fig 18 respectively.

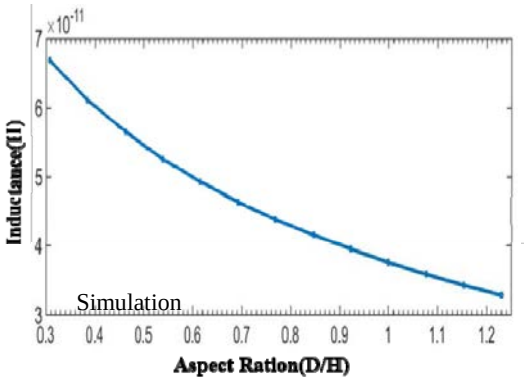


Figure. 15 Inductance of a signal TPV with varying aspect ratio

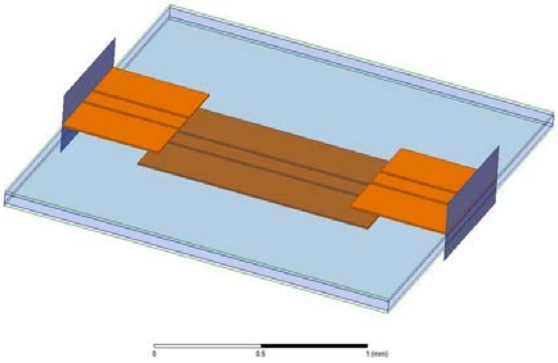


Figure.16 CPW based Dual Via Chain Structure

It can be observed that, as the diameter decreases the insertion loss reduces, though the resistance and inductance of each individual via increases. The increase in via impedance can be utilized to match to that of the transmission line, which is indicated through VSWR calculations in Fig 18. VSWR approaches a value of one as the via diameter decreases to 20 µm. These analyses indicate that 3dB bandwidth of structures based off TPVs can be increased with smaller via diameter and establishes the rationale behind the need for TPVs with smaller diameter, in the design of a 3D RF package.

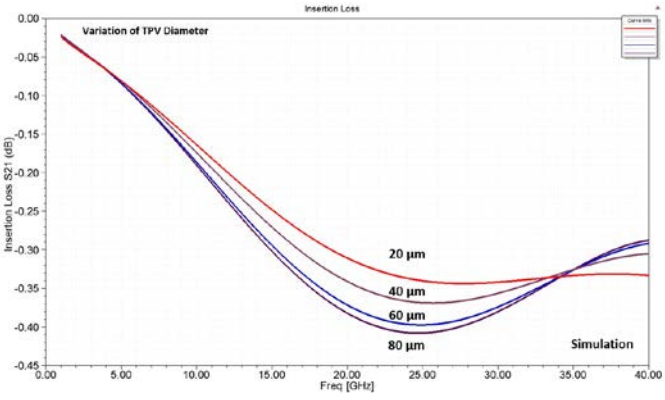


Figure.17 Insertion loss, S21 (dB), of CPW based Dual Via Chain, with varying via diameters

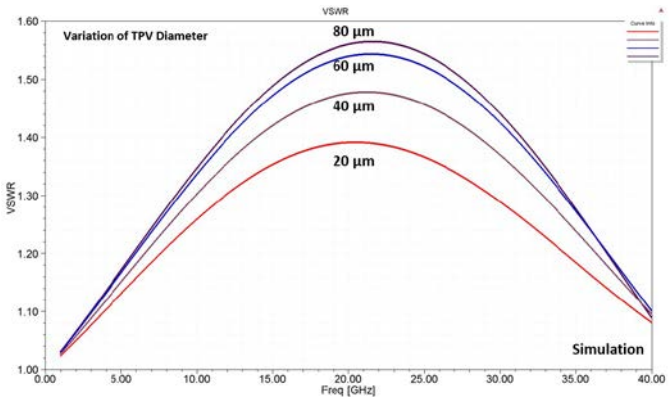


Figure.18 VSWR of CPW based Dual Via Chain with varying via diameters

V. Conclusions:

Increased I/O density, bandwidth, and improved signal integrity are the key requirements for 2.5D and 3D package systems. Fine-pitch TPVs are a key enabler for these high-performance packages. This paper reports the first comprehensive study on smaller via diameters in thinner glass substrates and validation of its superior thermomechanical and electrical performance. A novel substrate metallization technique, hereby named as primer process, and its optimization for fine TPVs on 100 µm thick glass substrate, was demonstrated. The impact of neighboring TPVs on the mechanical performance, at a pitch of 1.5x diameter, was estimated through Finite Element Analysis (FEA). In addition, the thermal reliability of TPVs structures in daisy chain pattern was validated through accelerated Thermal Cycle Test (TCT). The majority of TPV chains passed the reliability test with less than 15% change in DC resistance after 1000 cycles. A new methodology based off input impedance estimations was used to capture the parasitics of a single signal TPV. CPW based dual via chain structures with via transitions, was modelled using ANSYS HFSS™. Smaller diameter vias showed low insertion loss and VSWR. This establishes the rationale behind the need for smaller via diameters in 3D RF packages. Demonstration of superior reliability and electrical performance of ultra-small TPVs is a significant milestone towards the deployment of ultra-thin glass substrates for future 2.5D and 3D package architectures.

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