Dr. Nikita Ambasana

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Education

2017-Present Intel Tech. India Pvt. Ltd.

2012-2017 Indian Institute of Sciences, Bangalore, Ph.D
- CPI 7/8

2010-12 Dhirubhai Ambani Institute of Information and Communication Technology Gandhinagar (Gujarat)
M.Tech, Information and Communication Technology
- CPI 9.23/10

2005-09 Dharamsinh Desai Institute of Technology
Nadiad (Gujarat)
B.E., Electronics & Communication Engineering
- Aggregate 72.5%

Awards

Student Software Demonstration Prize, *IEEE Electrical Performance of Electronic Packages and Systems(EPEPS), 2015*, San Jose, CA, USA

Cisco Best Student Paper Award at *IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS), 2014,* Bangalore, India

Publications

N. Ambasana, G. Anand, D. Gope and B. Mutnury, "S-Parameter and Frequency Identification Method for ANN-Based Eye-Height/Width Prediction," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 7, no. 5, pp. 698-709, May 2017

N. Ambasana, G. Anand, B. Mutnury and D. Gope, "Eye-Height/Width Prediction from S-Parameters using Learning Based Models", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 6, No. 6, pp. 873-885, June 2016.

N. Ambasana, M. Sahu, D. Eesha, D. Gope and A. Chandrasekhar, “"Hybrid 2D-3D Fast Electromagnetic Analysis aided by Pattern Recognition for Signal Integrity Analysis”, Selected for presentation at *IEEE conference on Electric. Perf. of Electron. Packaging,* October 2019

N. Ambasana and D. Gope, "Mesh-sensitivity based decoupling capacitor sizing and placement for power delivery networks," *2017 IEEE 21st Workshop on Signal and Power Integrity (SPI)*, Baveno, 2017, pp. 1-4.

N. Ambasana,B. Nayak and D. Gope, " Mesh-based Impedance Sensitivity Formulation for DC/AC Power Integrity Design and Diagnosis", selected for presentation at *IEEE conference on Electric. Perf. of Electron. Packaging,* October 2016

D. Gope, G. Chatterjee, A. Das and N. Ambasana, "Smart Design Specific Electromagnetic Solvers for Chip-Package-Systems", to appear *Proc. IEEE Asia-Pacific Symposium on Electromagnetic Compatibility,* May 2016

Ambasana, N.; B. Mutnury and D. Gope, "Intelligent Rapid Investigation of S-parameters (IRIS)", (student software demonstration prize) *Proc. IEEE conference on Electric. Perf. of Electron. Packaging,* pp. 63-66, October 2015.

Ambasana, N.; Gope, D.; Mutnury, B.; Anand, G., “Automated Frequency Selection for Machine-Learning based EH/EW prediction from S-Parameters” (Selected for publishing in conference proceedings *Electrical Performance of Electronic Packaging and Systems (EPEPS), 2015*)

Ambasana, N.; Gope, D.; Mutnury, B.; Anand, G., "Eye-height/width prediction from S-Parameters using bounded size training set for ANN," *Electrical Design of Advanced Packaging & Systems Symposium (EDAPS), 2014 IEEE* , vol., no., pp.17,20, 14-16 Dec. 2014

Ambasana, N.; Gope, D.; Mutnury, B.; Anand, G., "Application of artificial neural networks for eye-height/width prediction from s-parameters," *Electrical Performance of Electronic Packaging and Systems (EPEPS), 2014 IEEE 23rd Conference on* , vol., no., pp.99,102, 26-29 Oct. 2014

Ambasana, N.; Gope, D.; Chandrasekhar, A., "Application of qualitative imaging methods to electrical performance-aware package board design," *Electrical Performance of Electronic Packaging and Systems (EPEPS), 2013 IEEE 22nd Conference on* , vol., no., pp.247,250, 27-30 Oct. 2013

Ambasana, N.B.; Zaveri, M., "Analysis of increased parallelism in FPGA implementation of neural networks for environment/noise classification and removal," *Engineering (NUiCONE), 2012 Nirma University International Conference on* , vol., no., pp.1,5, 6-8 Dec. 2012

Patents

B. Mutnury, G. Anand Burji, N. Ambasana, “Time domain response simulation system”, US10325043B2, United States, 2015

Patent filed on SWC Technology

Patents
Skills

Expertise Area	Power Integrity, Computational Electromagnetics, Signal Integrity, 3D & 2.5D Solvers (MoM), SPICE, Artificial Neural Networks
Programming Language	C, C++
Tools and Technologies	Sigrity PowerSI,PowerDC, RedHawk, Keysight ADS, Ansys HFSS, Q3D, HSPICE, MATLAB

Internship

Industrial	Dell Enterprise Server Group, Bangalore Guide: Dr. Bhyrav Mutnury Development of S-Parameter Analyzing & Envelope Viewer Tool in MATLAB	Mar'14-Nov'14
	e-Infochips, Ahmedabad Guide: Mr. Rahul Shah Training in Verification of ASIC designs using System Verilog and Perl scripting in LINUX	Dec'08 – April'09

Work Experience

Industry	PHED-DCG-DEG-Intel Tech India Pvt. Ltd.	
	Signal Integrity Engineer: Worked on next generation DDR and PCIe interfaces design and verification for reference platforms for next process technology nodes	Mar'17 – Jul'18
	Power Integrity Engineer: Worked on design and verification of power for memory rails with on board and in-chip VRs for latest technology nodes	Jul'18 - Present
	Worked on-chip power grid analysis and modeling	Sep'19 - Present
Academics	Teaching Assistant for the subjects Embedded Hardware Design and Digital Logic Design	Aug'10 – May'12
	Institute of Diploma Studies, Nirma University Position: Lecturer	Jun'09 – May'10

Positions of Responsibility

Treasurer for IEEE EPS Bangalore Chapter	Jan'19 – Present
Volunteer for EDAPS-2014	Oct'14 – Dec'14
Web Co-Chair for COMSNETS-2014	July'13 – Jan'14
Core Committee member of Sambhav (Social Service Group @ DA-IICT)	May'11 – May'12
Member of Cultural Committee, DDIT	Jul'06 – Apr'07
Head-Girl of St Ann's High School, Jamnagar	Jun'02 – Mar'03

Dt. 27th February, 2020