

Fanout and Embedded Packages: Recent Advances and Future Trends

Siddharth Ravichandran

3D Systems Packaging Research Center (PRC)

Georgia Tech, USA

Over the last decade, fanout and embedded packages have disrupted the entire semiconductor industry due to its benefits in size, cost, electrical & thermal performance, and potential for heterogeneous integration. Starting with RF System-in-Packages in the early 2010s, their scope and scale have dramatically changed since 2016 after being used in packaging Apple's A10 processor in iPhone 7. Today, fanout packages are driving a watershed in electronics packaging industry by eliminating wire bond and bump interconnections, underfills, and substrates across a variety of applications from low-cost consumer products to high-performance data center products.

This short course will introduce fanout and embedded packaging and cover some package structures, process flows, material & equipment challenges, design rules & benchmarking, along with some emerging trends in this field. Participants are not expected to have any background in semiconductor materials or processes to attend this course. At the end of this short course, we expect the participants to have a better understanding of the current state of the art in fanout and embedded packaging along with future trends including some of the work done by the Packaging Research Center (PRC) in this area.

Duration: 1.5 hours (including Q&A)

Bio of Siddharth Ravichandran:

Siddharth Ravichandran received his bachelor's in electrical engineering from College of Engineering, Guindy, India in 2013, and his master's in electrical and computer Engineering from Rutgers University, USA, in 2016. He is currently pursuing a Ph.D. in electrical engineering at the 3D Systems Packaging Research Center in Georgia Institute of Technology, USA. His Ph.D. research focusses on Glass-based embedded packages for a variety of applications.

He received the 2020 IEEE Electronics Packaging Society (EPS) Ph.D. fellowship award for his contributions to the development 2.5D and 3D glass packages for heterogeneous integration in high performance computing. He also received the 2019 IEEE EPS 'Future Packaging Vision' award at the 69th Electronics Components and Technology Conference (ECTC). His current research interests include heterogenous integration, 2.5D/3D architectures and advanced packaging for high-bandwidth & power-efficient applications.