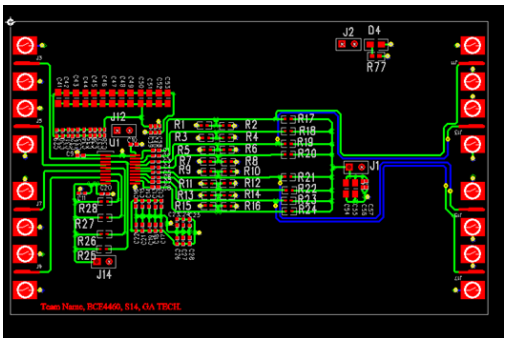
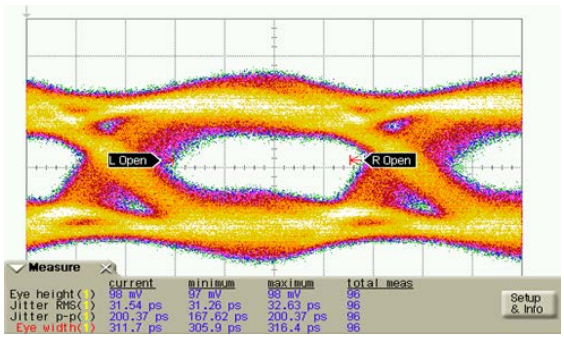
ECE 4460 – Introduction to Electronic Systems Packaging
(Offered Spring Semester)

Microelectronics represents a trillion dollar industry today where every electronic product requires integrated circuit chips and packaging to perform various functions. These products include personal computers, smart phones, wireless base stations, automobiles, super computers, IoTs and UAVs to name a few. A critical part of microelectronics is packaging without which the integrated circuits cannot communicate with each other and be connected to the external world. With the demand for light weight, small size, high performance and low cost systems, the role of packaging is becoming very important. *As the cost of monolithic integration is increasing there is a strong trend towards heterogeneous integration in the semiconductor industry which is all about packaging*.

This course provides an introduction to the history, challenges and opportunities arising in the packaging of electronic systems. *Electronic systems contain transistors interconnected together in the package and hence understanding electronic systems packaging cannot be complete without understanding the workings of the transistor and its interaction with the package*. The course therefore covers the basics associated with transistors, packaging, high speed signaling, power delivery, thermal management and packaging technologies. As part of this course, the students will work on projects for the design of packaged sub-systems using Physical CAD tools, parasitic extraction tools, and circuit simulators. Examples of work done by the students are shown in the figure below of a PCB design along with its measurements for maximizing signal and power integrity.



PCB Design



Measurement at 1Gbps

Prerequisites: ECE 3030 or ECE 3710 or ECE 3040

Reading Material:
1) Class Notes – *Posted on Canvas*.
2) Power Integrity Modeling and Design for Semiconductors and Systems, Madhavan Swaminathan and Ege Engin, Prentice Hall, 2007. ISBN0_13_615206_6
3) Fundamentals of Device and Systems Packaging: Technologies and Applications, Second Edition edited by Rao. R. Tummala, McGraw Hill, 2019. *This book can be downloaded from the library. Go to Databases – Access Engineering and search for the book title.*
4) Circuits, Interconnections and Packaging of VLSI, H. B. Bakoglu, Addison Wessley (Out of Print). *Select chapters posted on Canvas*.
5) Design and Modeling for 3D ICs and Interposers, Madhavan Swaminathan and KiJin Han, World Scientific Publishing Company, 2013. ISBN: 978_981_4508_59_9
6) K. S. Oh and X. Yuan, "High Speed Signaling: Jitter Modeling, Analysis and Budgeting", Prentice Hall, 2012.

Instructor: Madhavan Swaminathan, Pettit 109; Email: madhavan@ece.gatech.edu
Office Hours: TTh (3:30 – 5:00 pm) (or by appointment)

Please send email to Carol Mills for appointment (carol.mills@ien.gatech.edu)

TA:	Seunghyup Han, Klaus 1351; Email: (seunghyup@gatech.edu)
Room & Timing:	MWF 12:20pm – 1:10pm; VL C341
Website:	https://canvas.gatech.edu
Grading:	Homework (10%); Quiz1 (15%); Quiz 2 (15%); Project 1 (15%); Project 2 (25%); Final (20%)

Students will work in groups of two for Project 2 and individually for Project 1. The groupings will be assigned by the instructor. *Details on the project will be described later.*
All homework and project report should be neatly written and stapled. Points will be deducted unless this is followed. Any illegible homework submissions will get zero points.

Course Outcomes:

Upon successful completion of this course, students should be able to:

1) Explain the difference between ICs and Packaging
2) Calculate the impact of scaling on MOS Transistors and interconnects
3) Calculate the capacitance, resistance and RC delays of interconnects
4) Explain the fundamentals of packaging and different packaging technologies
5) Design and model transmission lines in package substrates (PCB)
6) Design H-Tree clock distribution networks
7) Explain the importance of power delivery networks for high speed signaling
8) Design and model power delivery networks on PCB
9) Explain the role of thermal management in high speed systems
10) Calculate thermal resistances for a system and resulting junction temperature for transistors
11) Design a PCB with ICs for high speed signaling that includes power delivery and make signaling and power supply noise measurements

Academic Integrity:
Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. Students are expected to act according to the highest ethical standards. For information on Georgia Tech's Academic Honor Code, please visit http://www.catalog.gatech.edu/policies/honor-code/ or http://www.catalog.gatech.edu/rules/18/. Any student suspected of cheating or plagiarizing on a quiz, exam, or assignment will be reported to the Office of Student Integrity, who will investigate the incident and identify the appropriate penalty for violations.

Student-Faculty Expectations Agreement:
At Georgia Tech we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. See http://www.catalog.gatech.edu/rules/22/ for an articulation of some basic expectation that you can have of me and that I have of you. In the end, simple respect for knowledge, hard work, and cordial interactions will help build the environment we seek. Therefore, I encourage you to remain committed to the ideals of Georgia Tech while in this class.

Tentative Course Outline for ECE 4460 – Spring '20
Meeting Place and Time: VL C341; MWF 12:20pm – 1:10pm
Professor: Madhavan Swaminathan (madhavan@ece.gatech.edu)

1/6 Course Review; ICs and Electronic Packaging
1/8 Microsystems Integration
1/10 Basics of High Speed Signaling
1/13 Logic to Memory Communication
1/15 Chip to Chip Communication
1/17 Device and Interconnect Scaling
1/20 Holiday (MLK Day) ☺
1/22 Device and Interconnect Scaling (cont.)
1/24 Interconnect Capacitance
1/27 Interconnect Capacitance (cont.)
1/29 Demo of Agilent ADS
1/31 Interconnect Capacitance (cont.)
2/3 Interconnect Resistance & RC Delays
2/5 Fundamentals of Packaging
2/7 Signal Transmission
2/10 **Quiz 1 ☹**
2/12 Transmission Lines and Matching
2/14 Transmission Lines and Matching (cont.)
2/17 Clock Distribution Basics
2/19 Clock Distribution Design
2/21 Interconnect Crosstalk
2/24 Channel Modeling & Design
2/26 Project 2 Details & Demo of PADS
2/28 Eye Diagrams
3/2 Power Delivery Engineering
3/4 Power Distribution Basics and Simple Relationships
3/6 Power Distribution Basics and Simple Relationships (cont.)
3/9 Concept of Target Impedance
3/11 Power Distribution Components: Switching Regulators
3/13 Power Distribution Components: Capacitors
3/16-20 Spring Break ☺
3/23 Power Distribution Components: Planes
3/25 Power Distribution Components: Low Drop-Out Regulator
3/27 Impedance calculations
3/30 Signaling and Power Supply Noise
4/1 Materials in Packaging
4/3 Quiz 2 ☹
4/6 Package Substrate Technologies
4/8 Chip & Package Assembly
4/10 Thermal Management
4/13 Thermal Management (cont.)
4/15 Thermo-mechanical reliability
4/17 3D Stacking & Packaging
4/20 Artificial Intelligence & Packaging
4/22 Reading Period
4/29 Final Exam (11:20am – 2:10pm) ☹

Note: Project 1 will be provided around 2/21/20. Details of Project 2 will be provided on 2/26/20. The tape out of the design for the project needs to be completed by 3/30/20 to enable fabrication. Assembly and measurements for the project will be done during the last week (4/20 - 4/22) or earlier. The final report for the project is due on 4/26/20 by 5pm. The instructor is expected to be

traveling on Feb 10, 12, 26, 28. During this time, the TA will teach the class. Parts of the material taught by the TA will be recovered by the instructor.